Explore Switches, Lights, and 7-Segments on DE2

The purpose of this exercise is to learn how to connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the switches *SW*17−0 on the DE2 board as inputs to the circuit. We will use light emitting diodes (LEDs).

The DE2 board provides 18 toggle switches, called *SW*17−0, that can be used as inputs to a circuit, and 18 red lights, called *LEDR*17−0, that can be used to display output values. Figure 1 shows a simple VHDL entity that uses these switches and shows their states on the LEDs. Since there are 18 switches and lights it is convenient to represent them as arrays in the VHDL code, as shown. We have used a single assignment statement for all 18 *LEDR* outputs, which is equivalent to the individual assignments

LEDR(17) <= SW(17);
LEDR(16) <= SW(16);
……
LEDR(0) <= SW(0);

The DE2 board has hardwired connections between its FPGA chip and the switches and lights. To use *SW*17−0 and *LEDR*17−0 it is necessary to include in your Quartus II project the correct pin assignments.
For example, the manual specifies that *SW*0 is connected to the FPGA pin *N25* and *LEDR*0 is connected to pin *AE23* (refer to the pin assignments *DE2 pin assignments.csv*).

The following file uses the names *SW*[0] …□*SW*[17] and *LEDR*[0] …□*LEDR*[17] for the switches and lights,

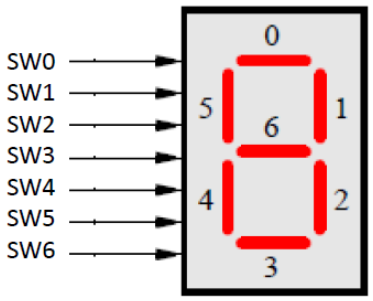
```
 1   LIBRARY ieee;
 2   USE ieee.std_logic_1164.all;
 3
 4   -- Simple module that connects the SW switches to the LEDR lights
 5   ENTITY Lab1 IS
 6       PORT (  SW      : IN    STD_LOGIC_VECTOR(17 DOWNTO 0);
 7               LEDR    : OUT   STD_LOGIC_VECTOR(17 DOWNTO 0));  -- red
     LEDs
 8   END Lab1;
 9
10   ARCHITECTURE Arc_Lab1 OF Lab1 IS
11   BEGIN
12       LEDR <= SW;
13   END Arc_Lab1;
14
```

-- LEDR <= SW; -- vector assignment
For line 12, you can replace LEDR <= SW with
LEDR(0) <= SW(0);

```
LEDR(1) <= SW(1);
…
LEDR(17) <= SW(17);
```

Perform the following steps to implement a circuit corresponding to the code on the DE2 board.

1. Create a new Quartus II project for your circuit. Select Cyclone II EP2C35F672C6 as the target chip, which is the FPGA chip on the Altera DE2 board.
2. Create a VHDL entity for the code in Figure 1 and include it in your project.
3. Include in your project the required pin assignments for the DE2 board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the switches and observing the LEDs.
5. Display a character on a 7-segment display. The seven segments in the display are identified by the indices 0 to 6 shown in the figure. Each segment is illuminated by driving it to the logic value 0. You are to write a VHDL module that implements logic functions that represent circuits needed to activate each of the seven segments. Connect the SW6, SW5, SW4, SW3, SW2, SW1, SW0 inputs to the HEX0 on your board. The The segments in this display are called $HEX0_0$, $HEX0_1$, : : :, $HEX0_6$. Making the required pin assignments, compile the project. (Refer to pin assignments from document posted)



9. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the SW6-0 switches and observing the 7-segment display.

10. Fill the following table while observing the 7-segment display.

SW6	SW5	SW4	SW3	SW2	SW1	SW0	Characters
1	0	0	0	0	0	0	**0**
1	1	1	1	0	0	1	**1**
0	1	0	0	1	0	0	**2**
							3
							4
							5

							6
							7
							8
							9
							F
							p
							g
							A

For your report:
The problem written in English
The flowchart to solve the problem
The design entry included (VHDL)
The pin assignment- assigning the circuit inputs and outputs to specific pins on the FPGA
The configuration for the FPGA Device (JTAG)
The test table you designed to record and verify the designed circuit on hardware
The conclusion