NEW YORK CITY COLLEGE OF TECHNOLOGY
THE CITY UNIVERSITY OF NEW YORK
Department of Computer Engineering Technology
300 Jay street, Brooklyn, NY 11201

CET 4805 Syllabus - Component and Subsystem Design II

Course Code: CET 4805

Course Title: Component and Subsystem Design II

Credits: 2 **Hours:** 3 lecture/laboratory/other

Catalog description:
Continuation of CET 4705. Further design of subsystems requiring solution by differential equations. Worst-case designs and component tolerances, development of control systems. A term project may be assigned.

Prerequisites: CET 4705 **Corequisites:** none

Reference Textbook:
Digital Electronics: A Practical Approach with VHDL (9th Edition), Kleitz, William, Prentice Hall, 2011, ISBN-13: 978-0132543033 | ISBN-10: 0132543036

Reference Books:
1. Digital Systems: Principles and Applications, 11/E, Ronald J. Tocci, Neal Widmer, Greg Moss, ISBN-10: 0135103827 • ISBN-13: 9780135103821, 2011 Prentice Hall
2. Rapid Prototyping of Digital Systems Quartus II Edition, Springer 2006 Hamblen, James O., Hall, Tyson S., Furman, Michael D. ISBN: 978-0-387-27728-8
3. Digital Systems Design Using VHDL , (second Edition), Charles H. Roth, Jr. and Lizy Kurian John, Thomson Publishing, 2008

Other Resources:
- Lecture Notes and Handouts and materials posted on Openlab at https://openlab.citytech.cuny.edu/wang-cet4805/
- Quick Start Guide Quartus II Software , Altera Corporation, http://www.altera.com/literature/manual/mnl_qts_quick_start.pdf, 2006
- DE2 Development and Educational User Board Users Manual, 2006.

Course Outcome:
The course provides an exciting and challenging laboratory component for implementation and testing of complex engineering projects. Each digital component and system design will come with integrated laboratory experimental activities. The prototyping of complex digital logic and software systems are used as a means to

demonstrate engineering practice and design. The course will introduce the students to basic design methodology, VHDL and CAD tools used in the design, synthesis and analysis of digital computer and communication systems, and Field-programmable gate array device **(**FPGAs). Upon successful completion of this course, the student will be able to use of the IEEE standard hardware description language (VHDL) and schematic design as practical means to implement hybrid sequential and combinational designs. Students will gain practical experience in the protocol, design, simulation and testing of digital systems. The Altera DE2 education board will provide the desired platform.

Topics Covered and Time Table:

1. Introduction to DE2 board and the Altera Quartus II Design Software and Simulation (schematic capture design and VHDL design) -
2. Programmable Logic Device of FPGAs. Getting Started with DE2 Board
3. VHDL Components and Port Maps
4. Design Code Character and Decoder. Programming FPGA board
5. Using BDF/VHDL Components in Digital Logic Design - Multi-bit Multiplexer and Programming a FPGA
6. Design the controlled character patterns and Programming a FPGA
   Midterm project week
7. Real time clock design, counter and frequency divider application
8. State Machine Design with VHDL
9. System design - Integrated components and subsystems.
10. Final project and final presentation

Project Report

Your project will be assigned and chosen based on the topic the course covered. The assignments will be posted on CUNY Blackboard. The project report will be conclusion

Grading Policy:

Embedded System Design projects and reports (40%)
Midterm (20%)
Final exam (or project) (35%)
Attendance (5%)
Project reports - Be graded based on the project report formative.
- No late submission will be accepted.
- All lab reports have to be submitted to the CUNY Blackboard on time.
- Any late submission will cause point deduction (50% deduction)

Grading Scale:	A=100%-93%	A-=90%-92.9%	B+=89.9%-87%
	B=86.9%-83%	B-=82.9%-80%	C+=79.9%-77%
	C=76.9%-70%	D=69.9%-60%	F=59.9% and below

Examination: There will have a mid-term examination. The examination date will be announced at later time. **There is NO make-up examination.**

Final: Final project will be presented on **Week 15**. A final date will be announced at later time. **There is NO make-up final**.

Academic Integrity: Students and all others who work with information, ideas, texts, images, music, inventions, and other intellectual property owe their audience and sources accuracy and honesty in using, crediting, and citing sources. As a community of intellectual and professional workers, the College recognizes its responsibility for providing instruction in information literacy and academic integrity, offering models of good practice, and responding vigilantly and appropriately to infractions of academic integrity. Academic dishonesty is prohibited in The City University of New York and is punishable by penalties, including failing grades, suspension, and expulsion.

Attendance: Under CUNY mandate, attendance in EACH class is REQUIRED and attendance will be taken at each class meeting. You are allowed a maximum of 2 absences. If you exceed that number, you may receive a WU grade. Excessive lateness (more than 15 minutes) will be considered to be an absence from that class meeting. Attendance will be counted as portion of your course grade. Each absent will be counted as 2% as portion of the course grade..

Classroom Policy: Any activity that threatens the CityTech's academic integrity will result in a disciplinary action. Such activities include, but are not limited to, inside or outside classroom cheating, copying others work in preparation of your own, giving or receiving information during quizzes, tests and final examination.

Course Instructor:
Dr. Yu Wang

Last Revised: Spring 2020

Notes:
The Instructor reserves the right to modify this outline anytime
All email communications must be from a CityTech email address, The subject line must include "CET4805" and your section number.