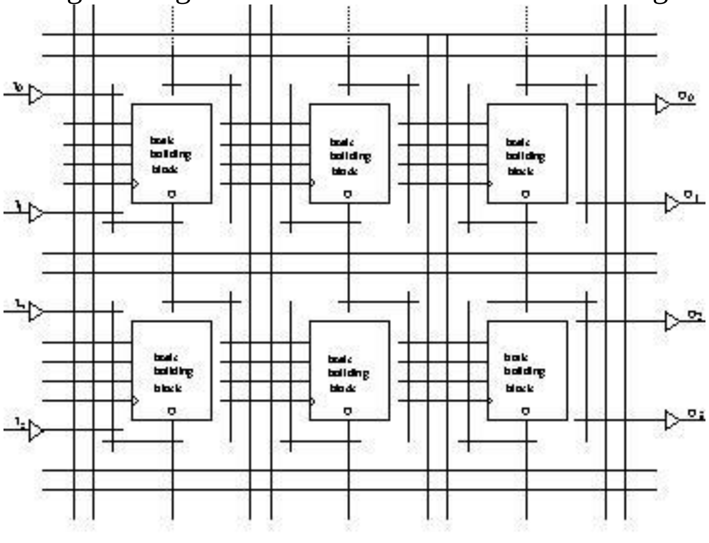
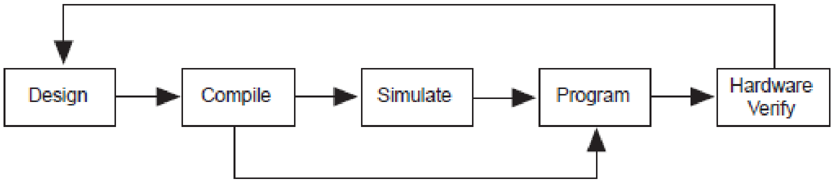
Introduction to Embedded Systems Design on FPGAs

Embedded system often refers to the non-PC systems which combines hardware and software design. The development of FPGA technology brings advantages to the embedded system in size, cost and performance. It is a hot application field which merges logic design and processor-based hardware development in a single or few chips solution. The merge of field programmable gate array (FPGA) technology and embedded system design have great influence on the traditional design methodology.

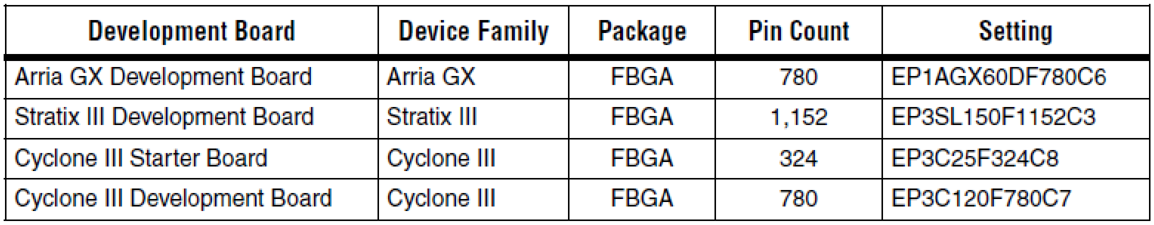


* Dashed lines are outputs from neighboring logic blocks which are not shown

An FPGA consists of an array of programmable logic blocks interconnected by programmable routing resources.



FPGA design flow



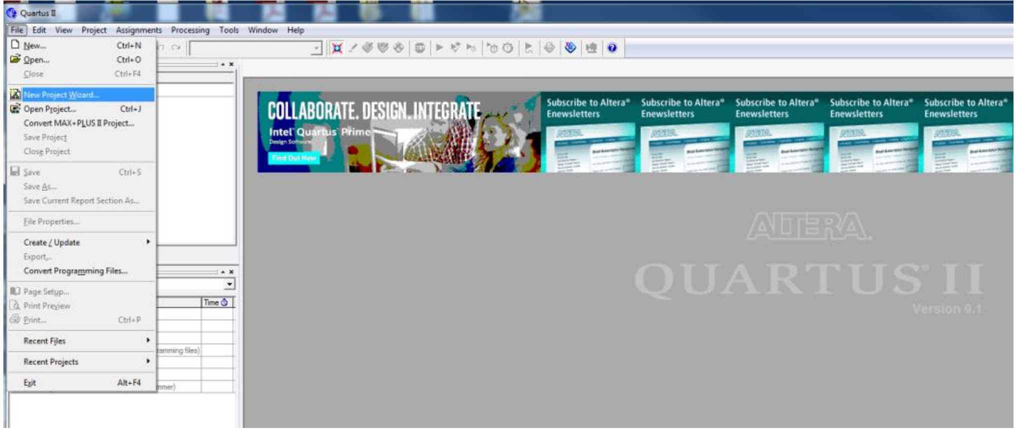
Development Board	Device Family	Package	Pin Count	Setting
Arria GX Development Board	Arria GX	FBGA	780	EP1AGX60DF780C6
Stratix III Development Board	Stratix III	FBGA	1,152	EP3SL150F1152C3
Cyclone III Starter Board	Cyclone III	FBGA	324	EP3C25F324C8
Cyclone III Development Board	Cyclone III	FBGA	780	EP3C120F780C7

Hands-on: FPGA design and run it on a FPGA development board

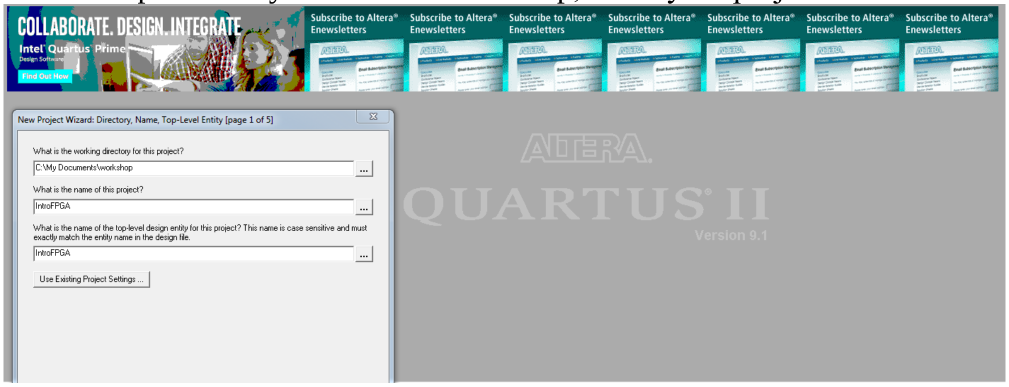
Implement a simple Boolean Equation X=AB+CD, and illustrate the steps involved to *design, simulate, and program a FPGA* using Altera's Quartus' II software.

A. Create a new project:

1) Create a new project:



2) Fill a name and top-level entity for the project.
Select path C:\My Documents\workshop, name your project "IntroFPGA"



New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]

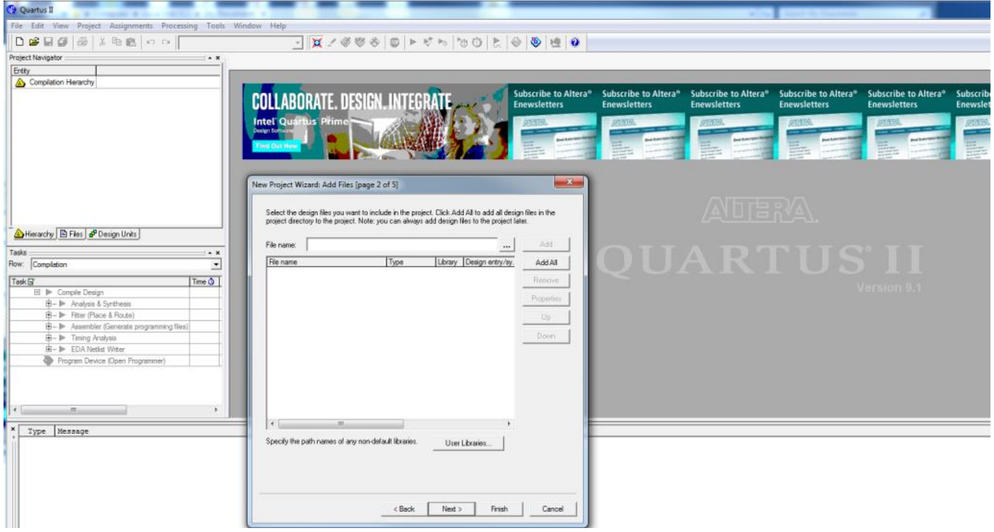
What is the working directory for this project?
C:\My Documents\workshop

What is the name of this project?
IntroFPGA

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
IntroFPGA

Use Existing Project Settings ...
COLLABORATE. DESIGN. INTEGRATE
Intel Quartus Prime
Find Out How
Subscribe to Altera® Enewsletters
ALTERA.
QUARTUS II
Version 9.1

3) Press Next

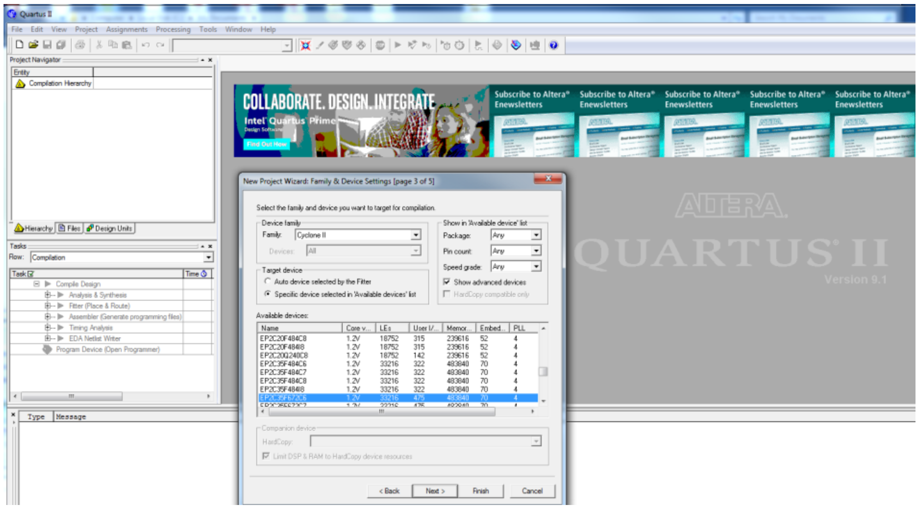


New Project Wizard: Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.

Specify the path names of any non-default libraries.

4) Select Cyclone II family, and choose EP2C35F672C6 which is the FPGA used on Altera’s DE2 board


New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone II

Devices: All

Show in 'Available device' list

Package: Any

Pin count: Any

Speed grade: Any

☑ Show advanced devices

□ HardCopy compatible only

Target device

○ Auto device selected by the Fitter

● Specific device selected in 'Available devices' list

Available devices:

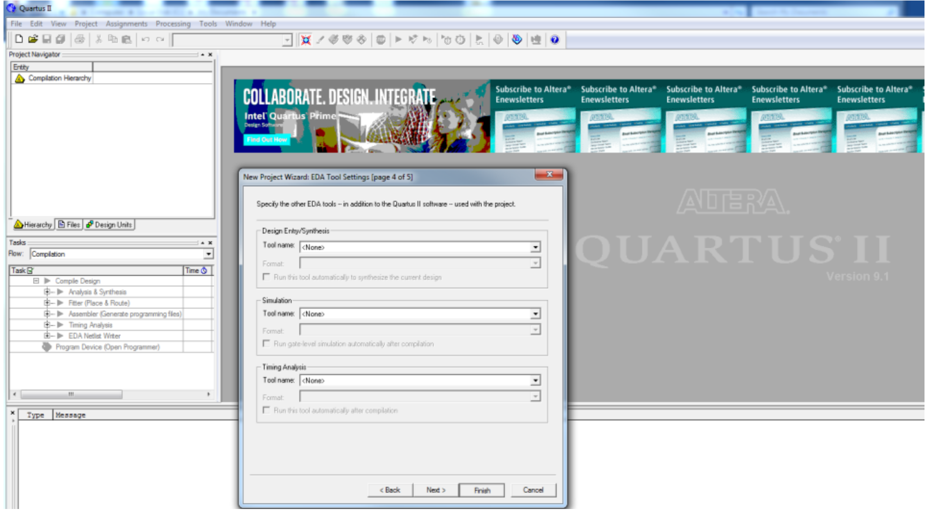
Name	Core v...	LEs	User I/...	Memor...	Embed...	PLL
EP2C20F484C8	1.2V	18752	315	239616	52	4
EP2C20F484I8	1.2V	18752	315	239616	52	4
EP2C20Q240C8	1.2V	18752	142	239616	52	4
EP2C35F484C6	1.2V	33216	322	483840	70	4
EP2C35F484C7	1.2V	33216	322	483840	70	4
EP2C35F484C8	1.2V	33216	322	483840	70	4
EP2C35F484I8	1.2V	33216	322	483840	70	4
EP2C35F672C6	1.2V	33216	475	483840	70	4

Companion device

HardCopy:

☑ Limit DSP & RAM to HardCopy device resources

5) Press Next and click Finish


New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

Design Entry/Synthesis

Tool name: <None>

Format:

□ Run this tool automatically to synthesize the current design

Simulation

Tool name: <None>

Format:

□ Run gate-level simulation automatically after compilation

Timing Analysis

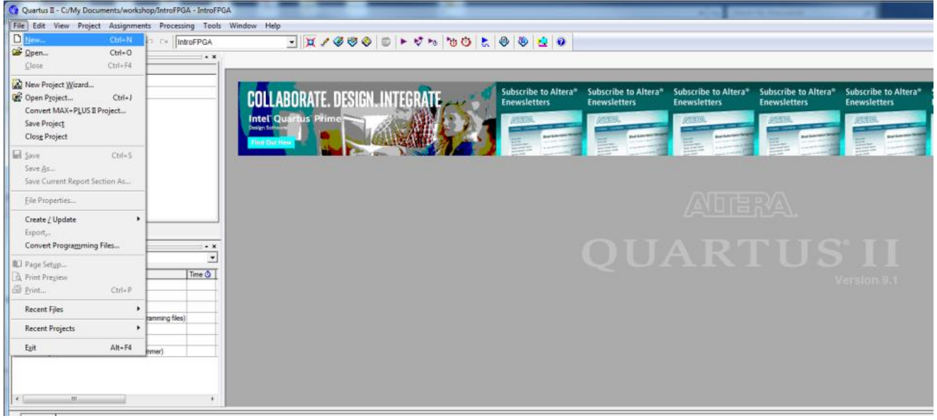
Tool name: <None>

Format:

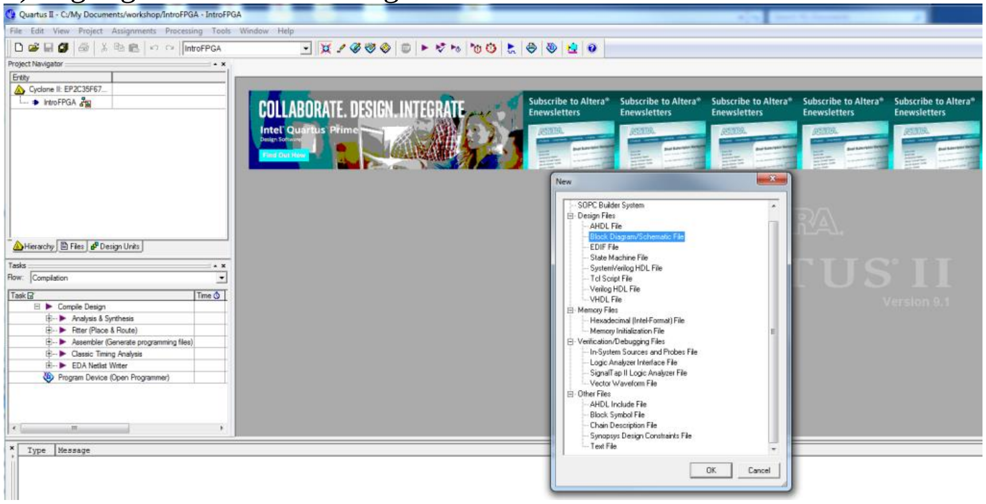
□ Run this tool automatically after compilation

B. Block Design File (bdf format)

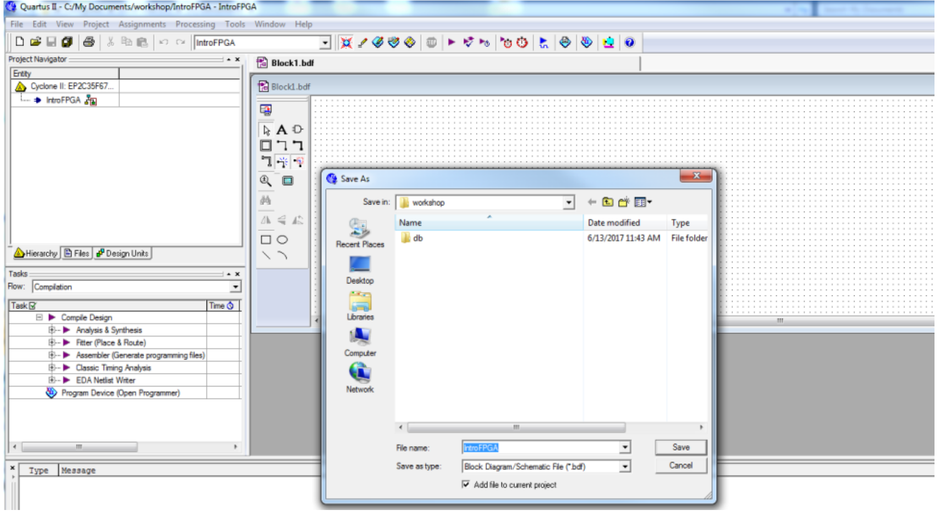
1) Choose New from File menu


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA

2) Highlight a new Block Diagram File



3) Choose Save As


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Block1.bdf
Save As
Save in: workshop
Recent Places
Desktop
Libraries
Computer
Network
Name
Date modified
Type
Save
Cancel

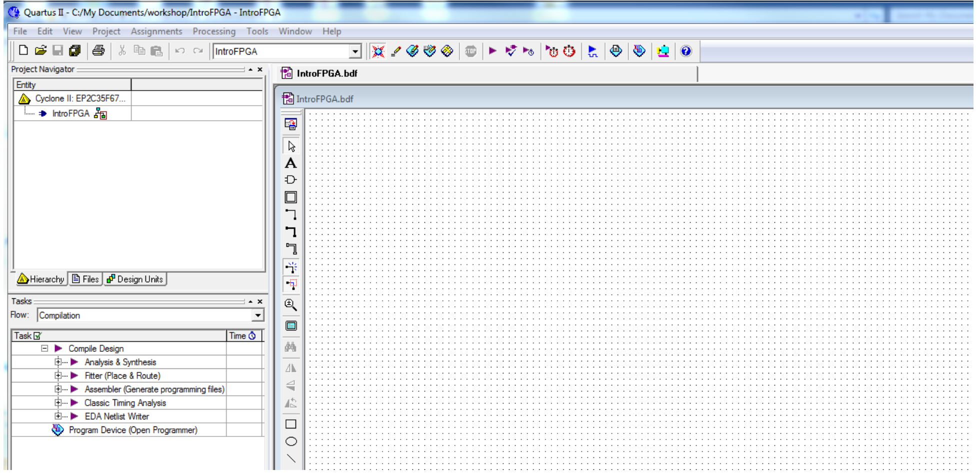
Name	Date modified	Type
db	6/13/2017 11:43 AM	File folder

File name: IntroFPGA

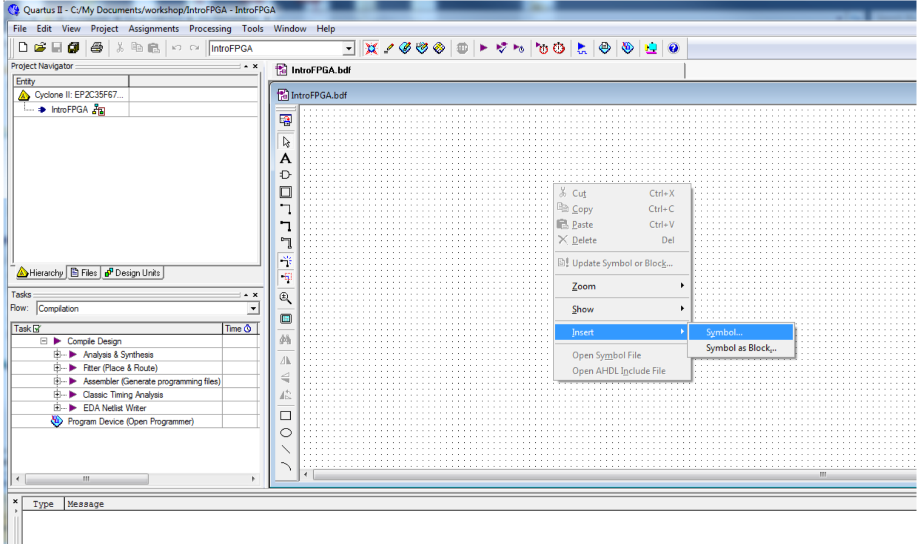
Save as type: Block Diagram/Schematic File (*.bdf)

☑ Add file to current project

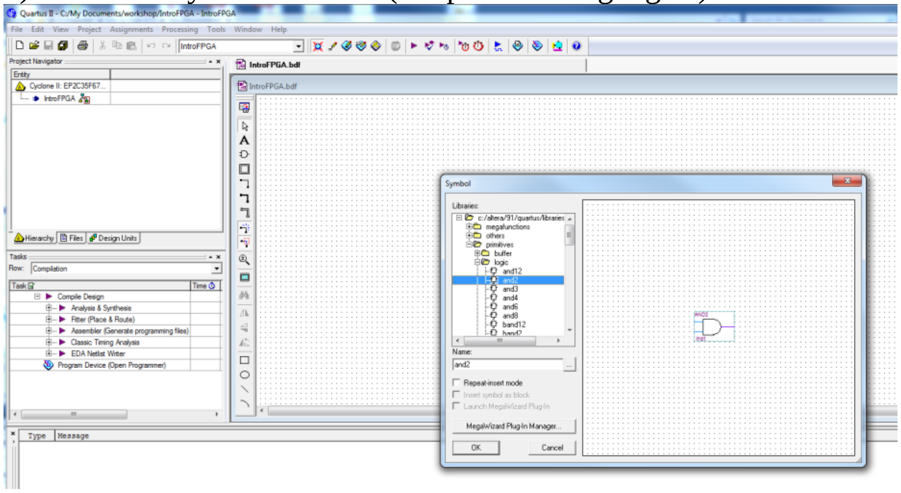
4) Enter the file name of IntroFPGA and press Save



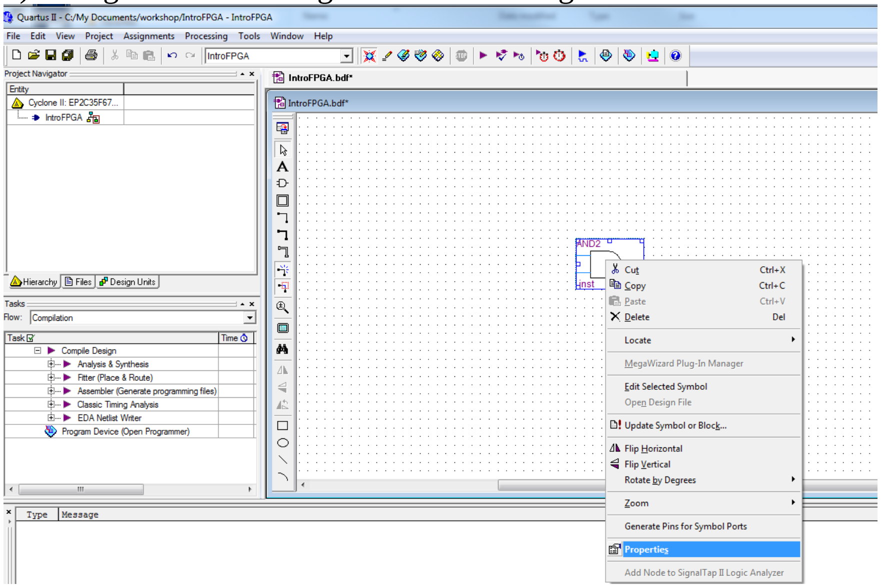
5) Right click the mouse in the empty workspace

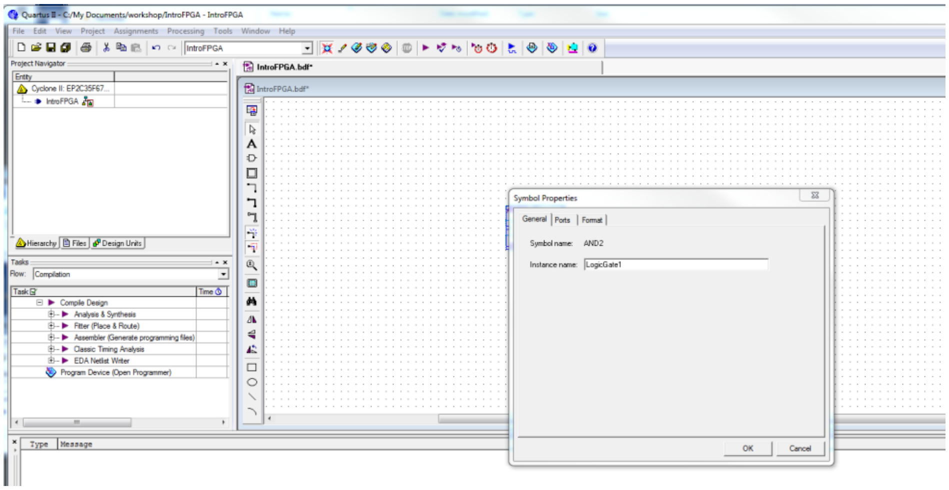


6) Insert -> Symbol of **and2** (2 input AND logic gate)



7) Assign the name “LogicGate1” to and2 gate


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
IntroFPGA.bdf*
AND2
inst
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Delete Del
Locate
MegaWizard Plug-In Manager
Edit Selected Symbol
Open Design File
Update Symbol or Block...
Flip Horizontal
Flip Vertical
Rotate by Degrees
Zoom
Generate Pins for Symbol Ports
Properties
Add Node to SignalTap II Logic Analyzer
Type
Message

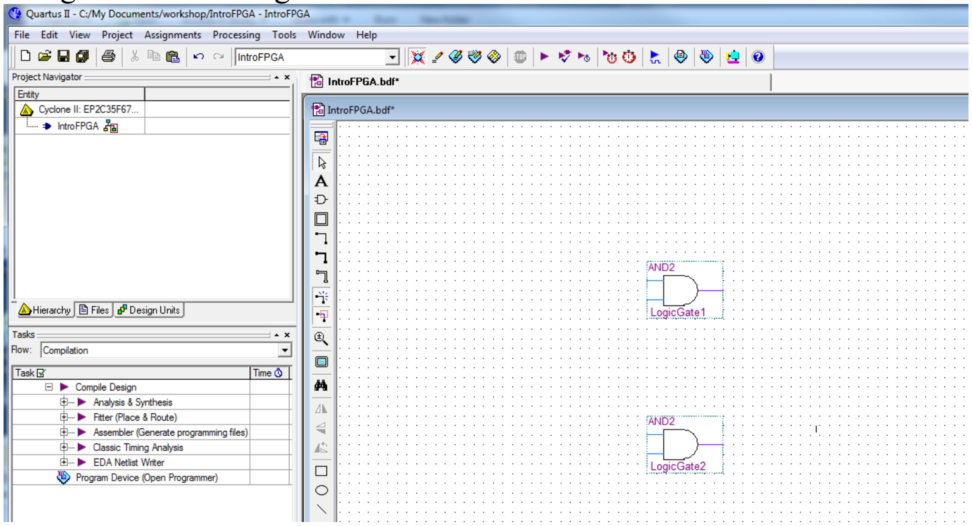


Symbol Properties

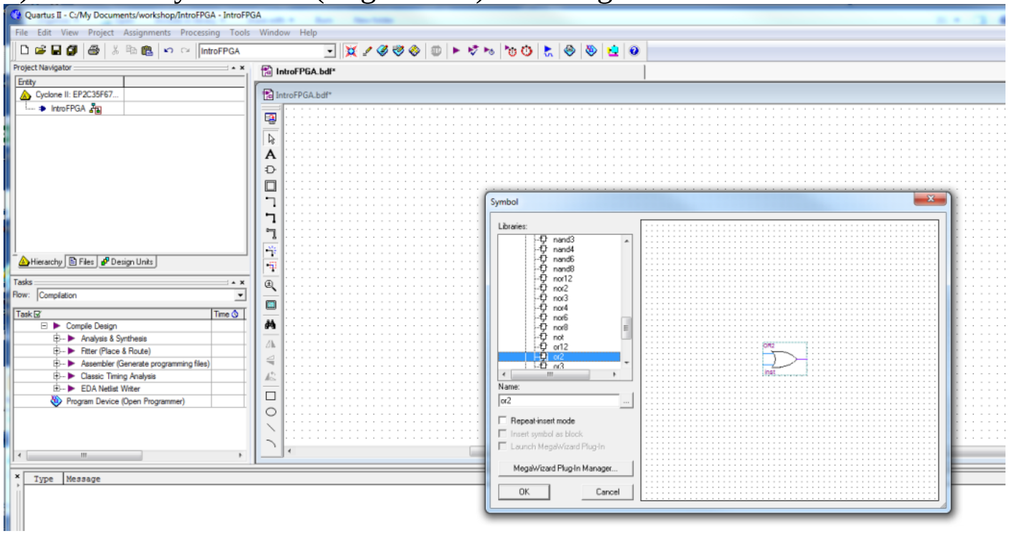
Symbol name: AND2

Instance name: LogicGate1

7) Repeat steps of 5) and 6) and insert a symbol and2
Assign the name "LogicGate2" to and2



8) Insert -> Symbol or2 (LogicGate3) and assign the name



Symbol

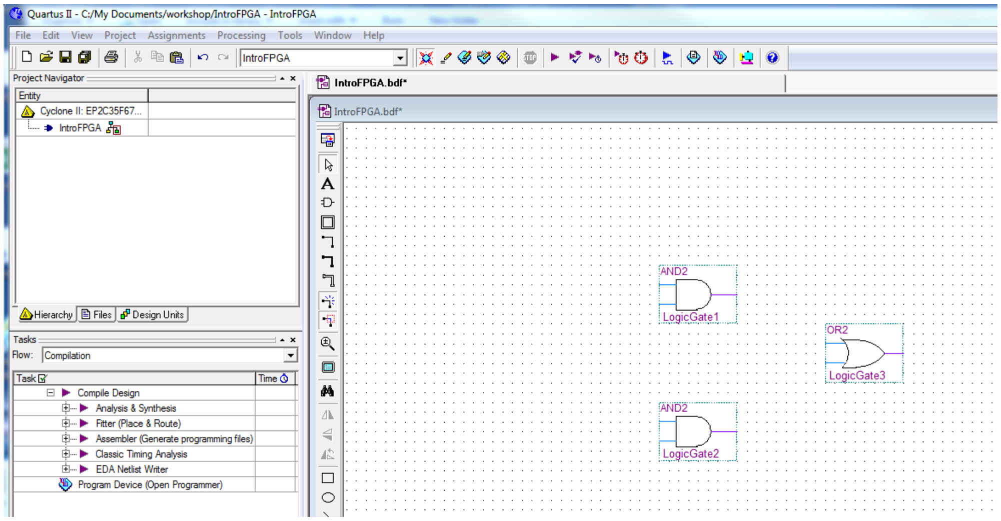
Name: or2

□ Repeat-insert mode

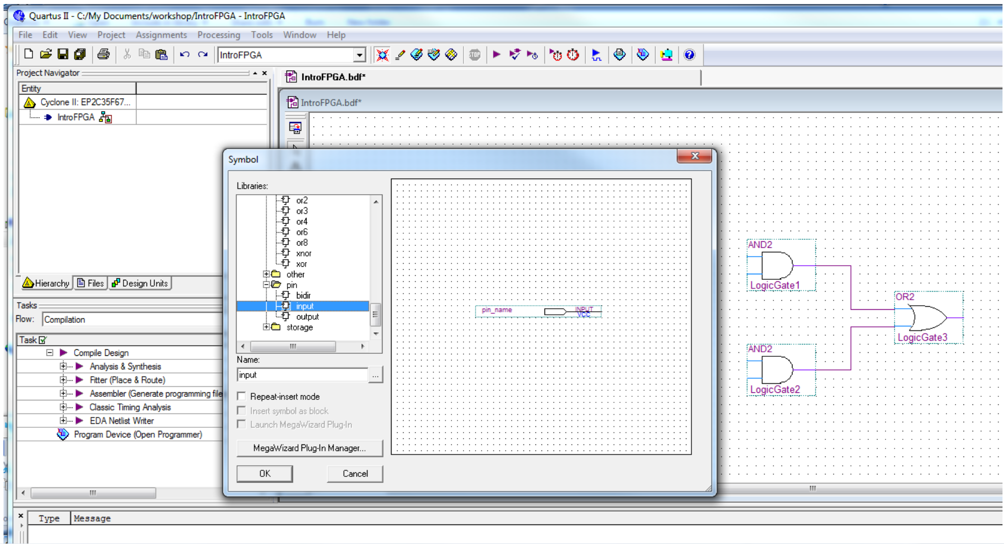
□ Insert symbol as block

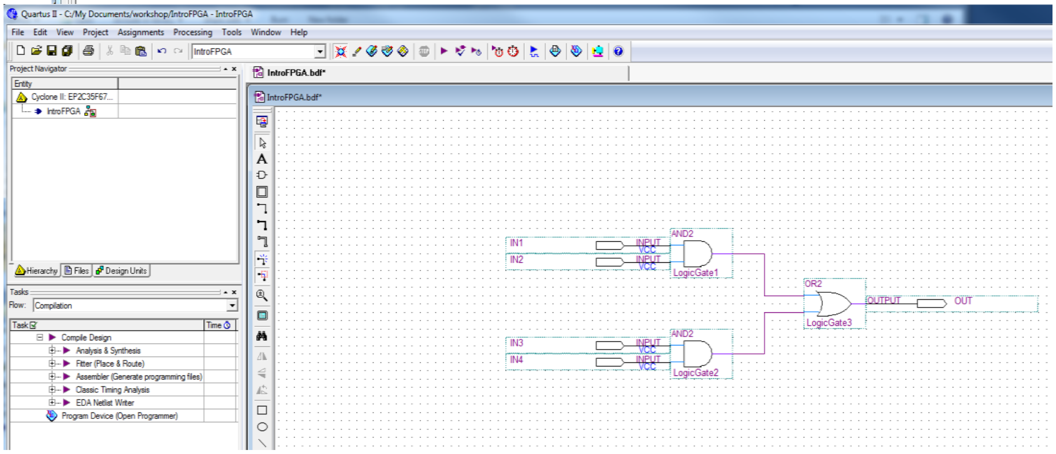
□ Launch MegaWizard Plug-In

Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
Libraries:
nand3
nand4
nand6
nand8
nor12
nor2
nor3
nor4
nor6
nor8
not
or12
or2
or3
MegaWizard Plug-In Manager...
OK
Cancel

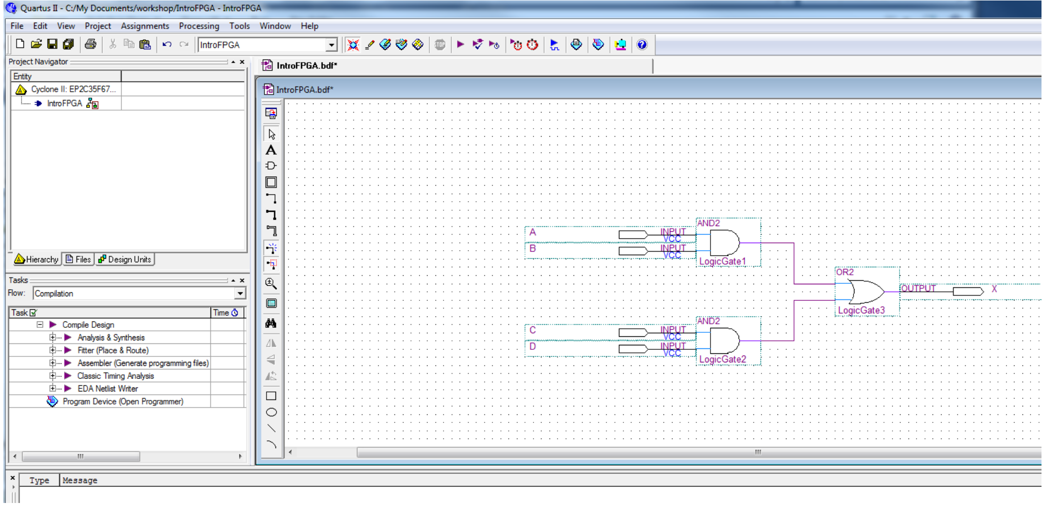


9) Make wire connection and insert input/output pin to implement X=AB + CD. The bdf workspace now has gates of AND and OR, and 4 input pins and 1 output pin. Then make circuit connections.



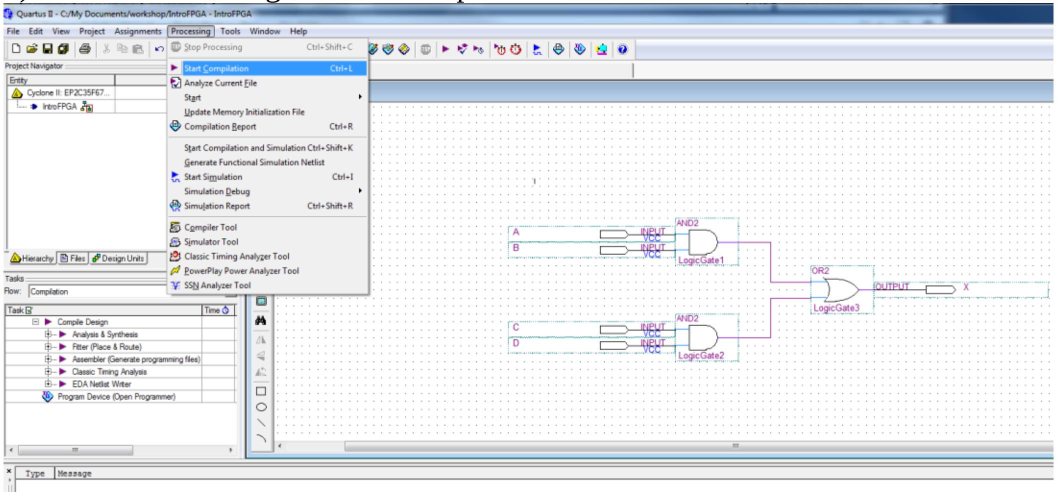


10) Change input and output terminal name to A, B, C, D, and X, respectively.

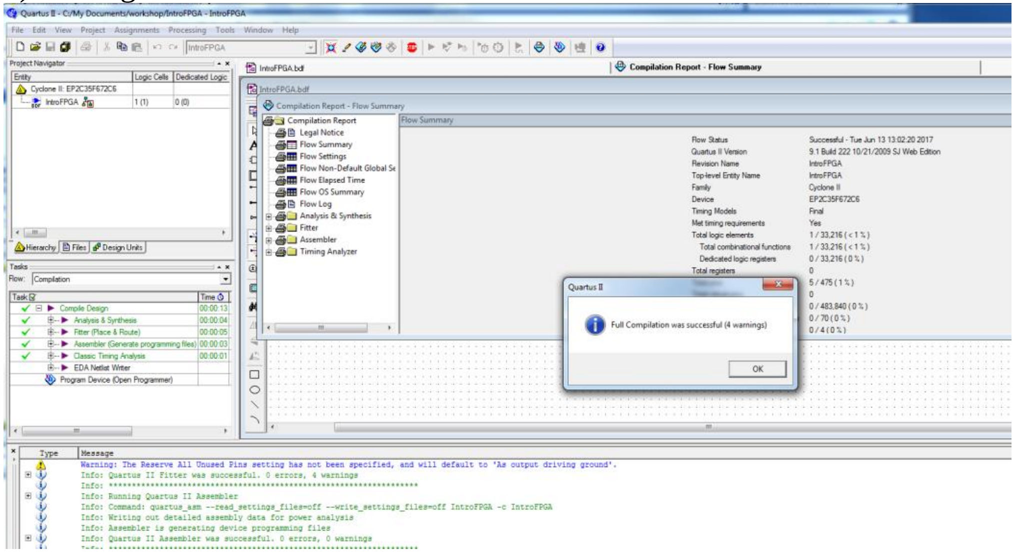


C. Compiling the project

1) Choose Processing -> Start Compilation


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation and Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Project Navigator
Entity
Cyclone II: EP2C35F67...
IntroFPGA
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
A
B
C
D
INPUT
VCC
AND2
LogicGate1
LogicGate2
OR2
LogicGate3
OUTPUT
X
Type
Message

2) Message indicated no error


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA
Project Navigator
IntroFPGA.bdf
Compilation Report - Flow Summary
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Se
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Quartus II
Full Compilation was successful (4 warnings)
OK
Hierarchy
Files
Design Units

Entity	Logic Cells	Dedicated Logic
Cyclone II: EP2C35F672C6		
IntroFPGA	1 (1)	0 (0)

Flow: Compilation

Task	Time
✓ Compile Design	00:00:13
✓ Analysis & Synthesis	00:00:04
✓ Fitter (Place & Route)	00:00:05
✓ Assembler (Generate programming files)	00:00:03
✓ Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

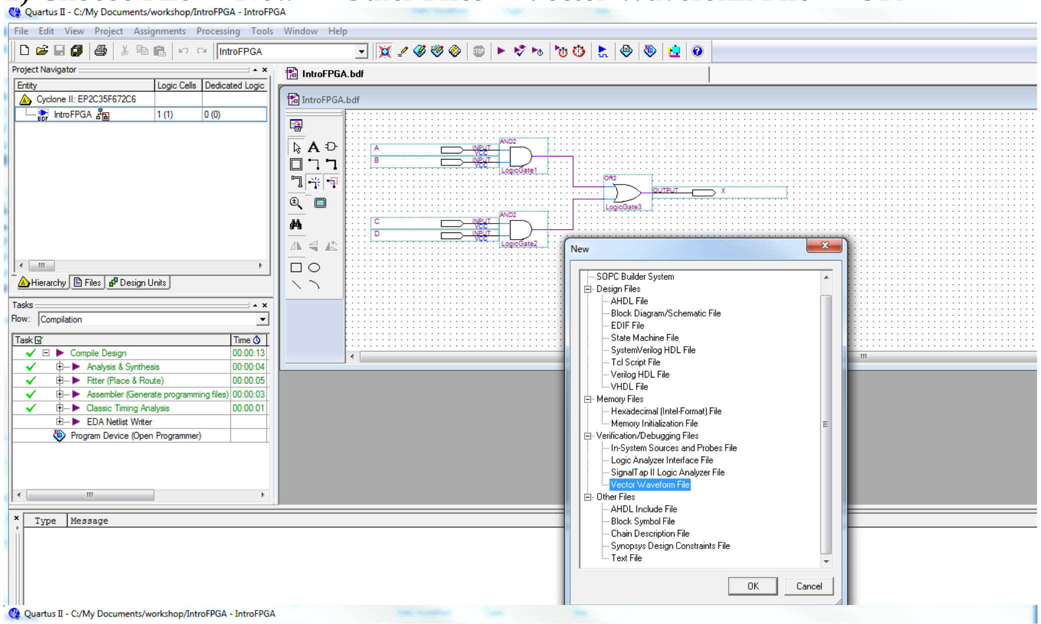
Flow Summary

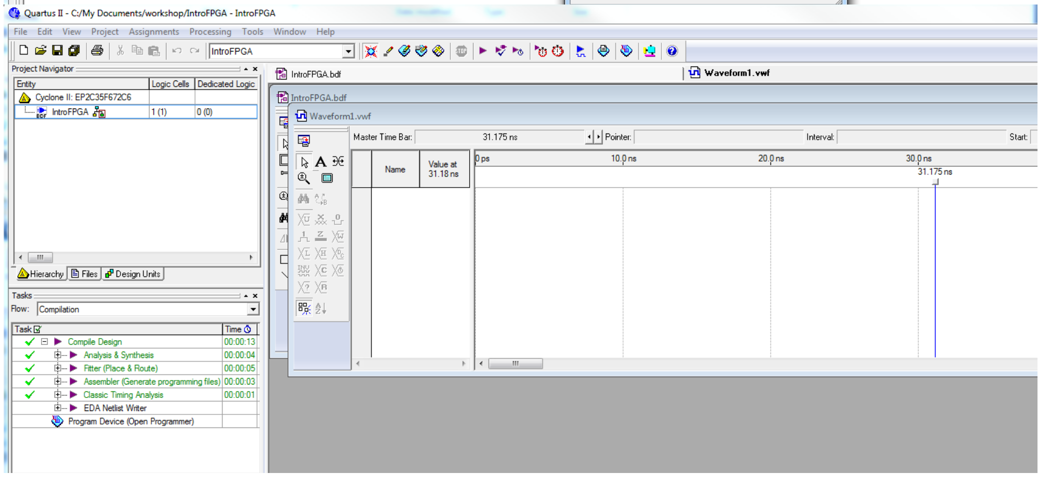
Flow Status	Successful - Tue Jun 13 13:02:20 2017
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	IntroFPGA
Top-level Entity Name	IntroFPGA
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
[illegible]	5 / 475 (1 %)
[illegible]	0
[illegible]	0 / 483,840 (0 %)
[illegible]	0 / 70 (0 %)
[illegible]	0 / 4 (0 %)

```
Type  Message
      Warning: The Reserve All Unused Pins setting has not been specified, and will default to 'As output driving ground'.
      Info: Quartus II Fitter was successful. 0 errors, 4 warnings
      Info: *******************************************************************
      Info: Running Quartus II Assembler
      Info: Command: quartus_asm --read_settings_files=off --write_settings_files=off IntroFPGA -c IntroFPGA
      Info: Writing out detailed assembly data for power analysis
      Info: Assembler is generating device programming files
      Info: Quartus II Assembler was successful. 0 errors, 0 warnings
      Info: *******************************************************************
```

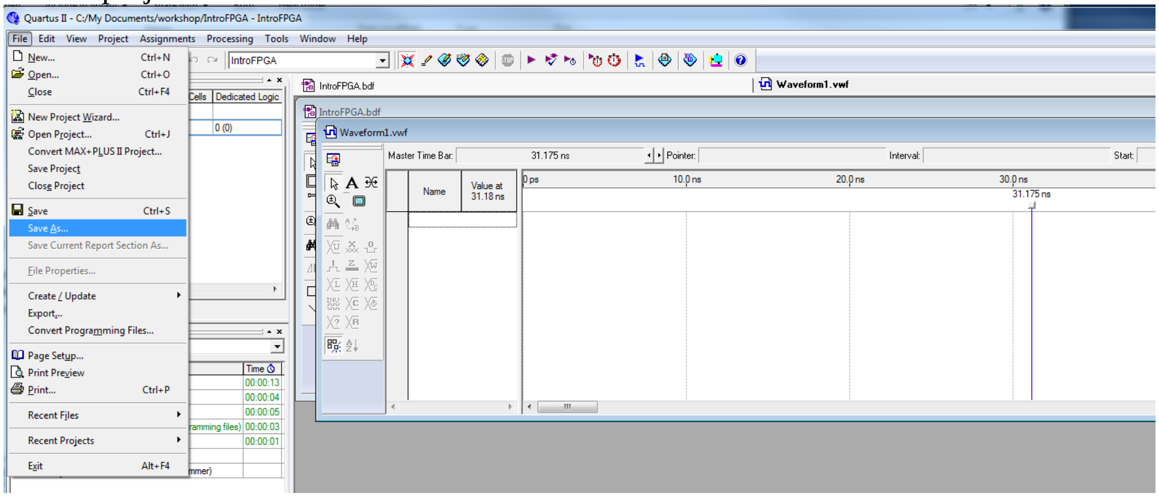
D. Create a Vector Waveform File (vwf) to simulate the design

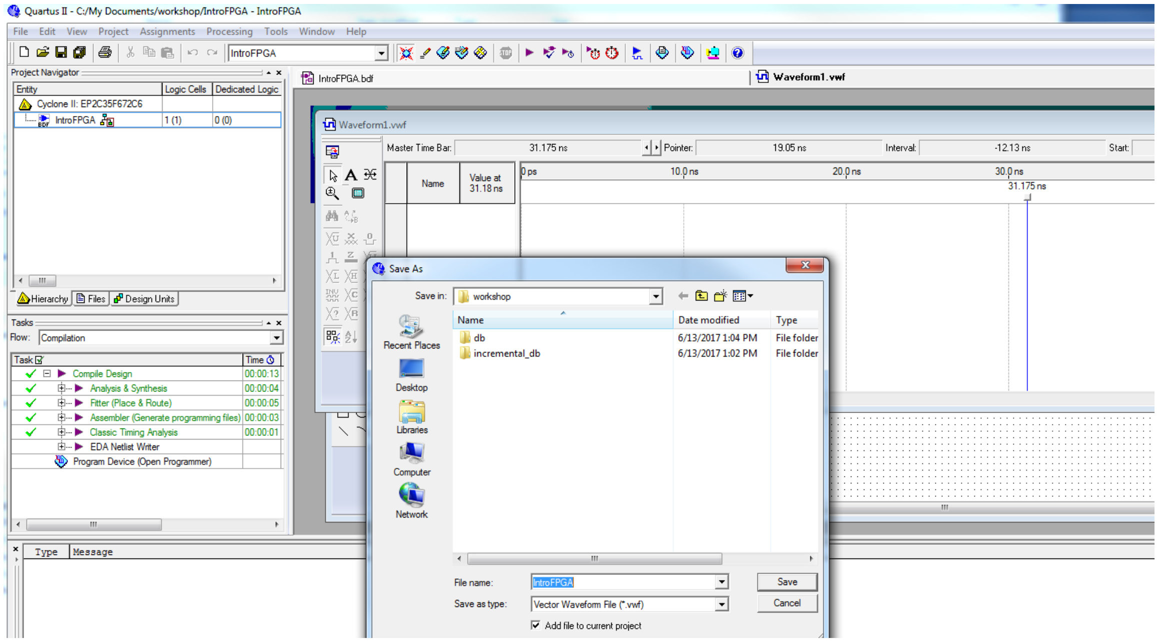
1) Choose File -> New -> Other Files ->Vector Waveform File -> OK


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA.bdf
New
SOPC Builder System
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
SignalTap II Logic Analyzer File
Vector Waveform File
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel



2) Save the vector waveform file (wvf) as IntroFPGA. Check the box of Add file to current project





Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA

Entity	Logic Cells	Dedicated Logic
Cyclone II: EP2C35F672C6		
IntroFPGA	1 (1)	0 (0)

Flow: Compilation

Task	Time
✓ Compile Design	00:00:13
✓ Analysis & Synthesis	00:00:04
✓ Fitter (Place & Route)	00:00:05
✓ Assembler (Generate programming files)	00:00:03
✓ Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

Waveform1.vwf — Master Time Bar: 31.175 ns Pointer: 19.05 ns Interval: -12.13 ns

Save As — Save in: workshop

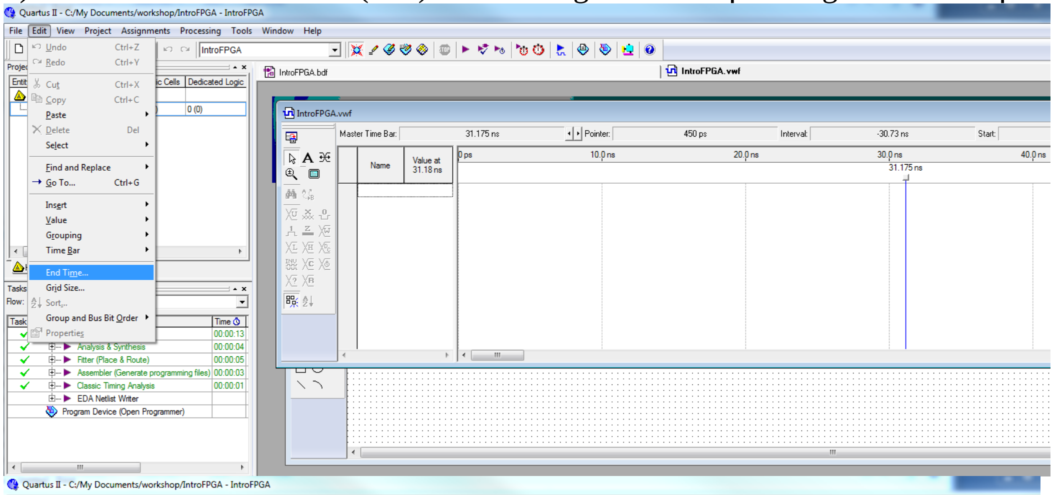
Name	Date modified	Type
db	6/13/2017 1:04 PM	File folder
incremental_db	6/13/2017 1:02 PM	File folder

File name: IntroFPGA

Save as type: Vector Waveform File (*.vwf)

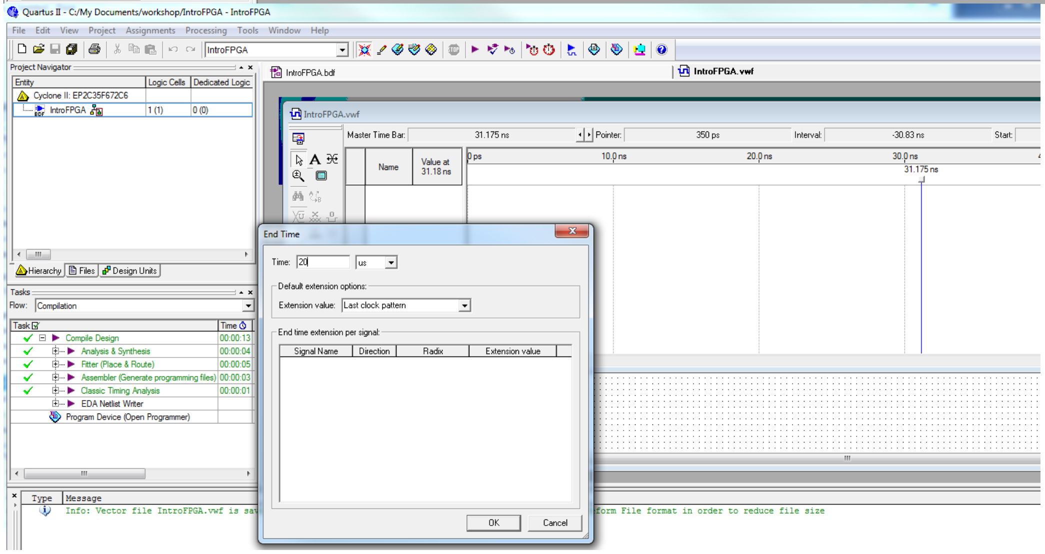
☑ Add file to current project

3) Build the simulation file (vwf) with ending time of 20μs and grid size of 1 μs



Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA

IntroFPGA.vwf — Master Time Bar: 31.175 ns Pointer: 450 ps Interval: -30.73 ns



Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA

IntroFPGA.vwf — Master Time Bar: 31.175 ns Pointer: 350 ps Interval: -30.83 ns

End Time

Time: 20 us

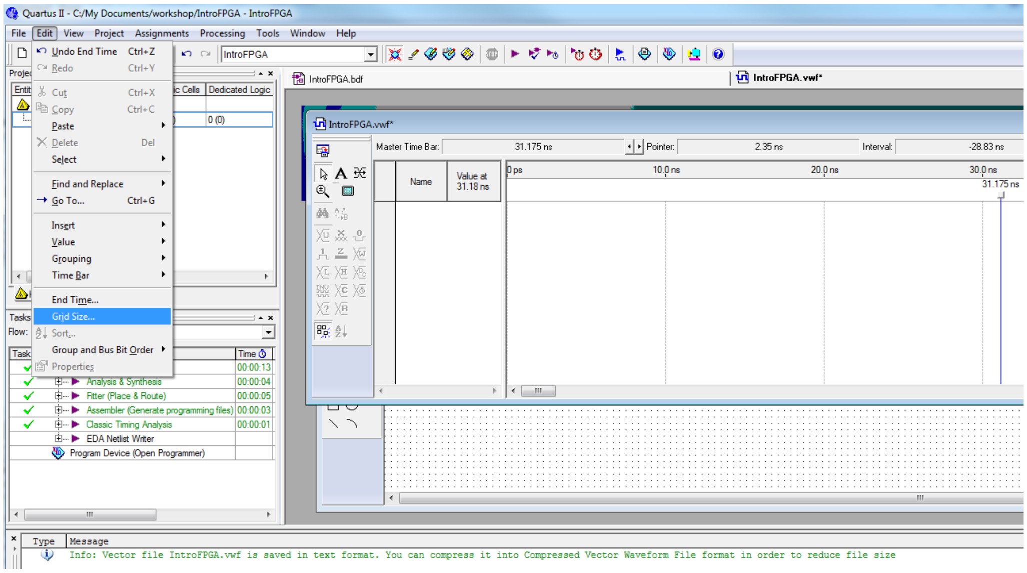
Default extension options:

Extension value: Last clock pattern

End time extension per signal:

Signal Name	Direction	Radix	Extension value

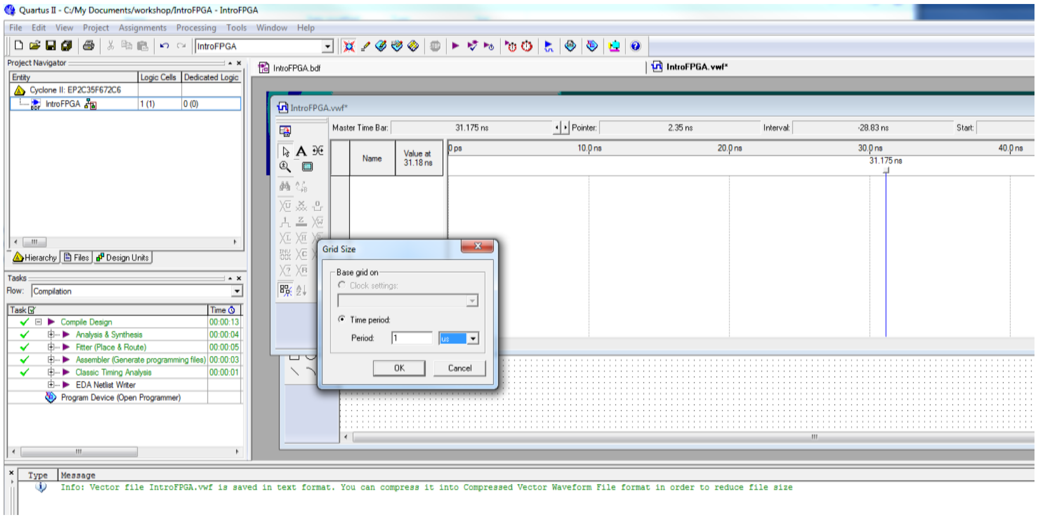
Info: Vector file IntroFPGA.vwf is sa... ...form File format in order to reduce file size



Master Time Bar: 31.175 ns Pointer: 2.35 ns Interval: -28.83 ns

Task	Time
Analysis & Synthesis	00:00:04
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

```
Info: Vector file IntroFPGA.vwf is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
```


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Files
Design Units
IntroFPGA.bdf
IntroFPGA.vwf*
Grid Size
OK
Cancel

Entity	Logic Cells	Dedicated Logic
Cyclone II: EP2C35F672C6		
IntroFPGA	1 (1)	0 (0)

Master Time Bar: 31.175 ns Pointer: 2.35 ns Interval: -28.83 ns

Base grid on

○ Clock settings:

● Time period:

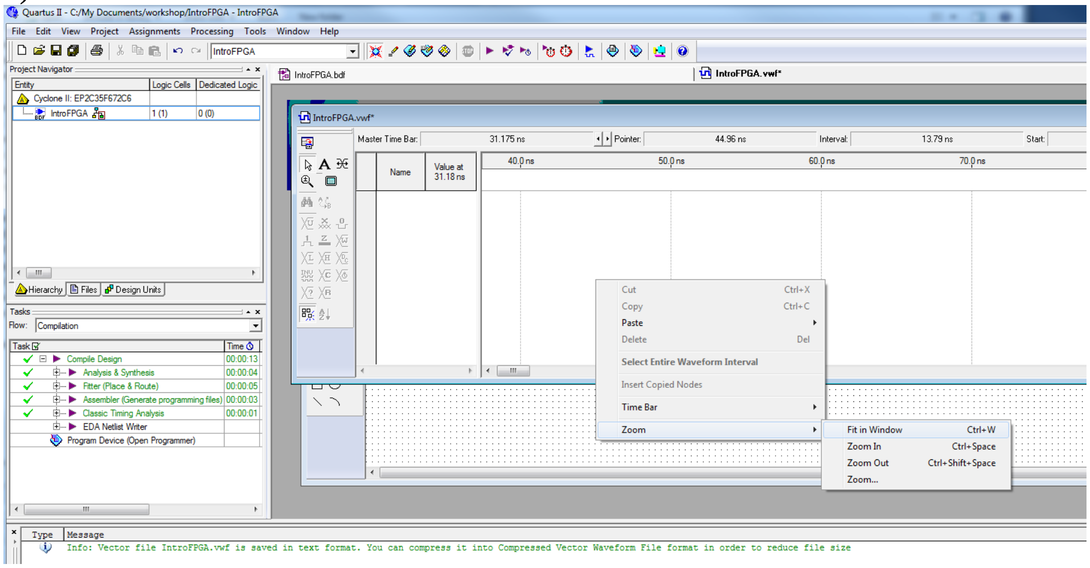
Period: 1 us

Flow: Compilation

Task	Time
Compile Design	00:00:13
Analysis & Synthesis	00:00:04
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

```
Info: Vector file IntroFPGA.vwf is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
```

4) View -> Fit in Window



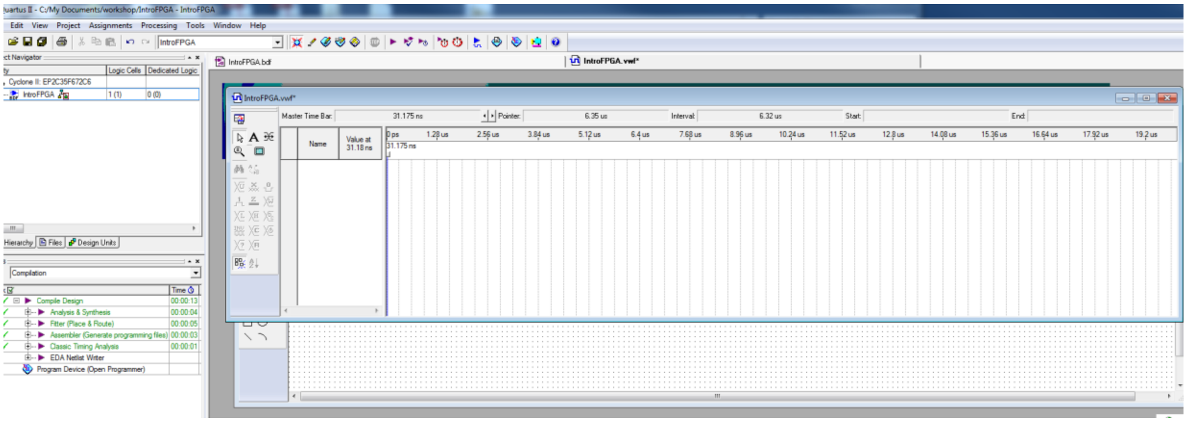
Entity	Logic Cells	Dedicated Logic
Cyclone II: EP2C35F672C6		
IntroFPGA	1 (1)	0 (0)

Master Time Bar: 31.175 ns Pointer: 44.96 ns Interval: 13.79 ns

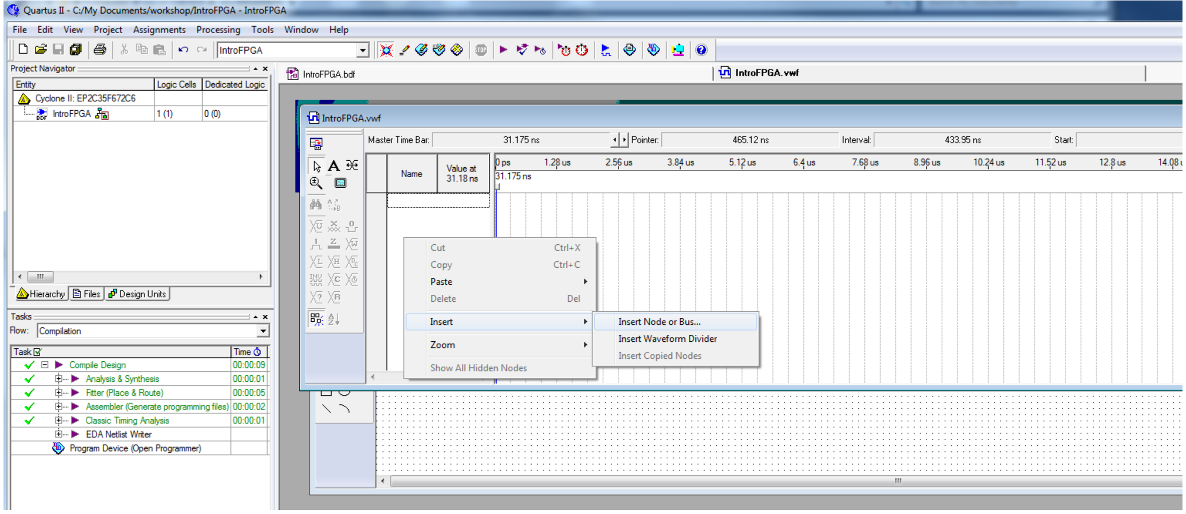
Flow: Compilation

Task	Time
Compile Design	00:00:13
Analysis & Synthesis	00:00:04
Fitter (Place & Route)	00:00:05
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

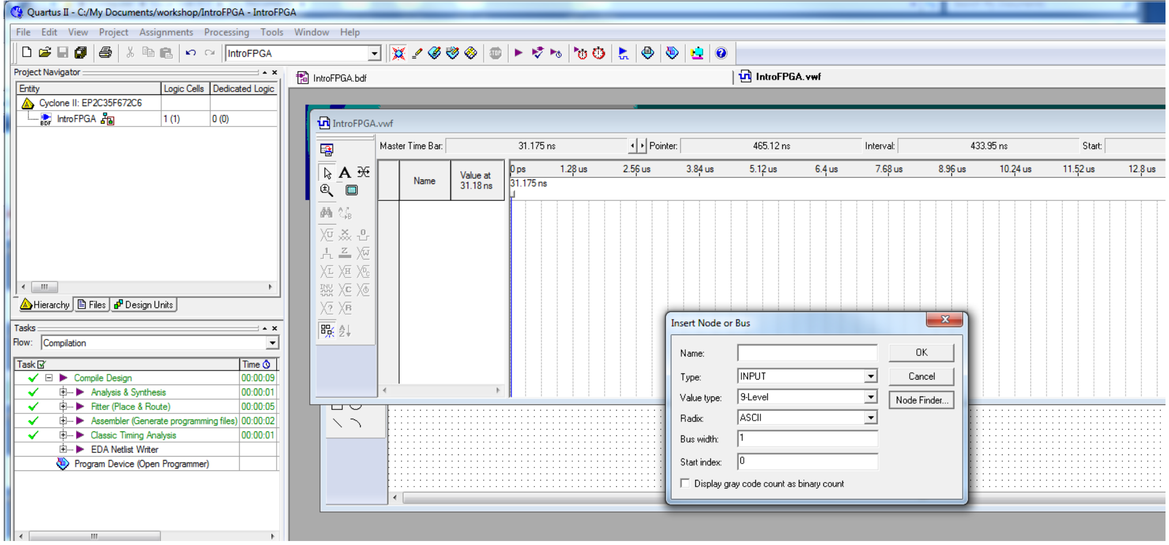
```
Info: Vector file IntroFPGA.vwf is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
```



6) Add inputs and outputs to the waveform (vwf)
Right click and select Insert Node or Bus

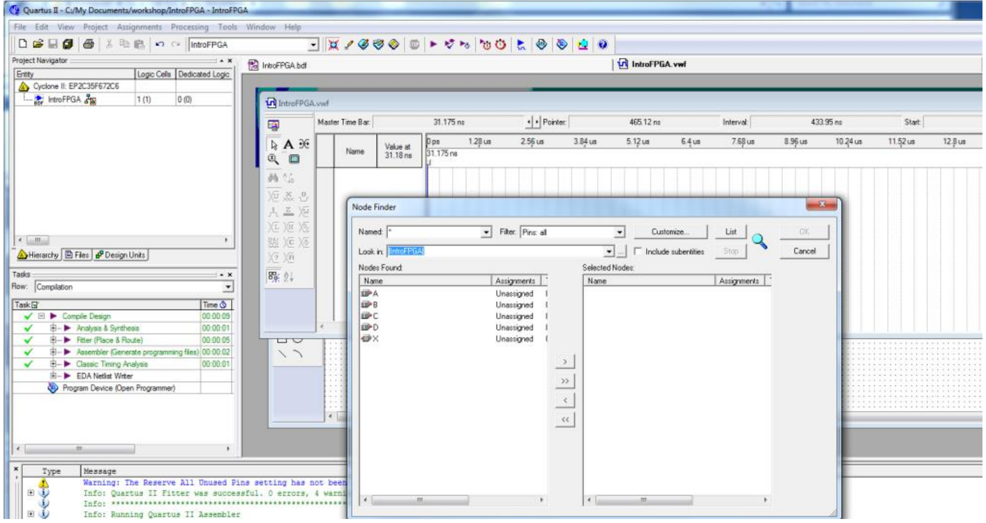


7) Click Node Finder



Name:
Type: INPUT
Value type: 9-Level
Radix: ASCII
Bus width: 1
Start index: 0
□ Display gray code count as binary count

6) Choose Filter: Design Entry (All Name)


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA.bdf
IntroFPGA.vwf
Node Finder
Customize...
List
OK
Cancel
Stop
Include subentities
Hierarchy
Files
Design Units

Named: *
Filter: Pins: all
Look in: |IntroFPGA|

Nodes Found:

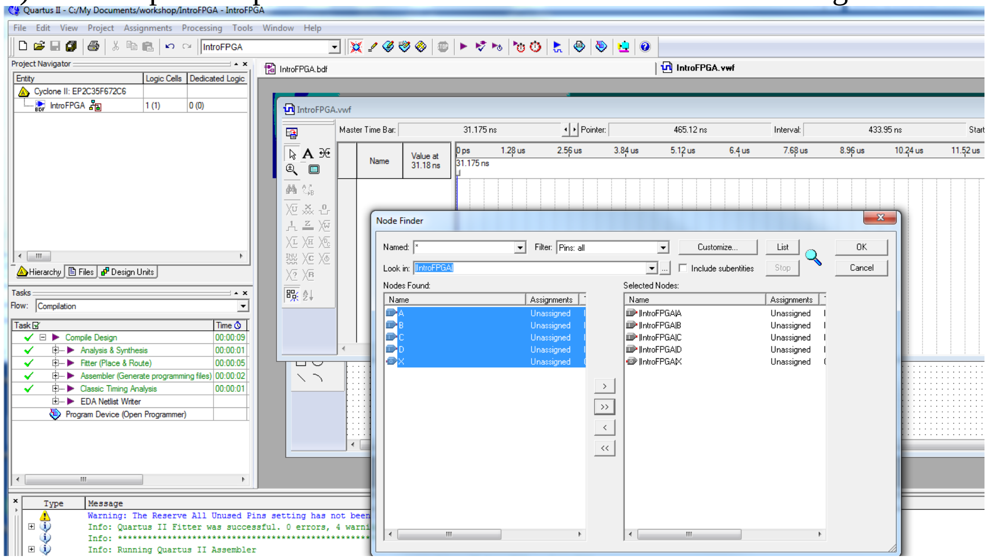
Name	Assignments
A	Unassigned
B	Unassigned
C	Unassigned
D	Unassigned
X	Unassigned

Selected Nodes:

Name	Assignments

```
Warning: The Reserve All Unused Pins setting has not been
Info: Quartus II Fitter was successful. 0 errors, 4 warni
Info: ***********************************************
Info: Running Quartus II Assembler
```

7) Select inputs/outputs names from Node Finder screen to the right side and click OK


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA.bdf
IntroFPGA.vwf
Node Finder
Customize...
List
OK
Cancel
Stop
Include subentities

Named: *
Filter: Pins: all
Look in: |IntroFPGA|

Nodes Found:

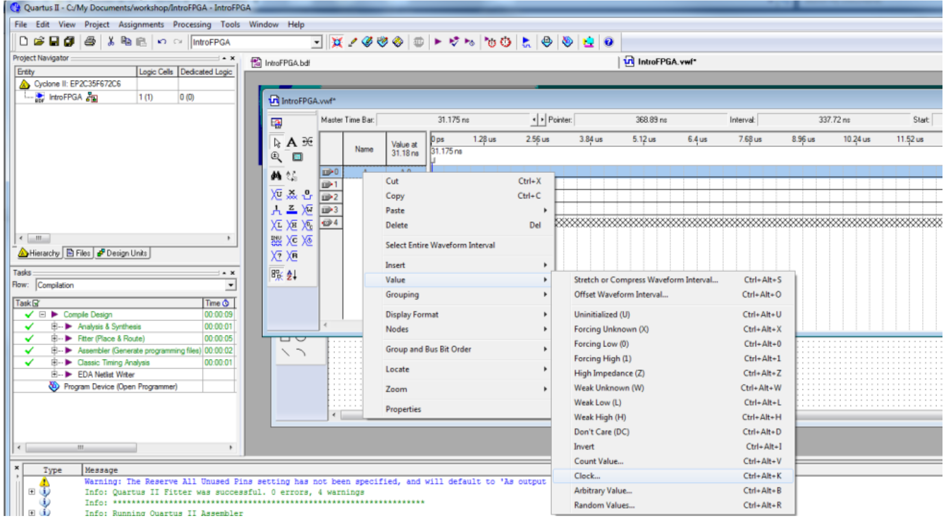
Name	Assignments
A	Unassigned
B	Unassigned
C	Unassigned
D	Unassigned
X	Unassigned

Selected Nodes:

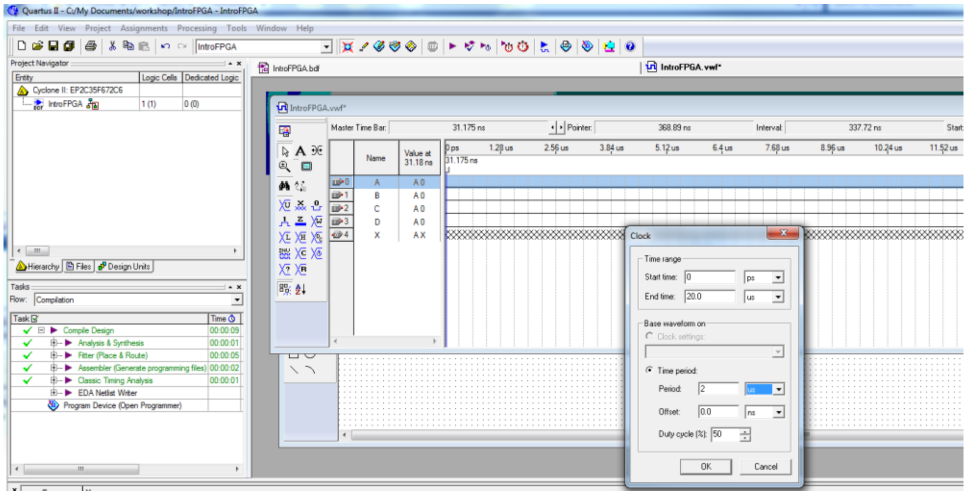
Name	Assignments
|IntroFPGA|A	Unassigned
|IntroFPGA|B	Unassigned
|IntroFPGA|C	Unassigned
|IntroFPGA|D	Unassigned
|IntroFPGA|X	Unassigned

```
Warning: The Reserve All Unused Pins setting has not been
Info: Quartus II Fitter was successful. 0 errors, 4 warni
Info: ***********************************************
Info: Running Quartus II Assembler
```

8) Highlight the input A, choose Edit =>Value =>Clock. Enter a period of 2µs, press Ok


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA.bdf
IntroFPGA.vwf*
Cut Ctrl+X
Copy Ctrl+C
Paste
Delete Del
Select Entire Waveform Interval
Insert
Value
Grouping
Display Format
Nodes
Group and Bus Bit Order
Locate
Zoom
Properties
Stretch or Compress Waveform Interval... Ctrl+Alt+S
Offset Waveform Interval... Ctrl+Alt+O
Uninitialized (U) Ctrl+Alt+U
Forcing Unknown (X) Ctrl+Alt+X
Forcing Low (0) Ctrl+Alt+0
Forcing High (1) Ctrl+Alt+1
High Impedance (Z) Ctrl+Alt+Z
Weak Unknown (W) Ctrl+Alt+W
Weak Low (L) Ctrl+Alt+L
Weak High (H) Ctrl+Alt+H
Don't Care (DC) Ctrl+Alt+D
Invert Ctrl+Alt+I
Count Value... Ctrl+Alt+V
Clock... Ctrl+Alt+K
Arbitrary Value... Ctrl+Alt+B
Random Values... Ctrl+Alt+R

```
Warning: The Reserve All Unused Pins setting has not been specified, and will default to 'As output
Info: Quartus II Fitter was successful. 0 errors, 4 warnings
Info: *********************************************************************
Info: Running Quartus II Assembler
```



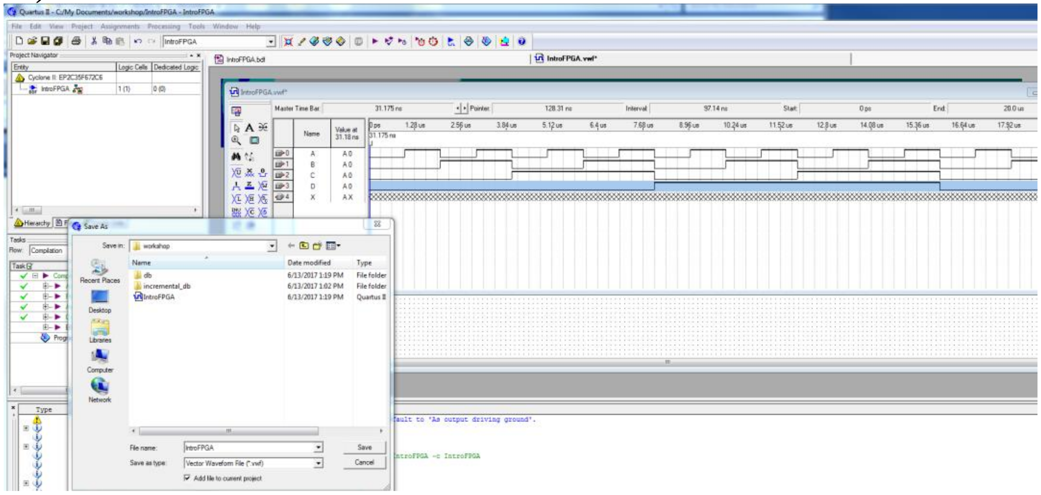
Time range
Start time: 0 ps
End time: 20.0 us
Base waveform on
○ Clock settings:
● Time period:
Period: 2 us
Offset: 0.0 ns
Duty cycle (%): 50
OK Cancel

9) Highlight the input B, choose Edit =>Value =>Clock. Enter a period of 4µs, press OK

10) Highlight the input C, choose Edit =>Value =>Clock. Enter a period of 8µs, press Ok

11) Highlight the input D, choose Edit =>Value =>Clock. Enter a period of 16µs, press Ok

12) Choose File => Save as IntroFPGA.vwf file



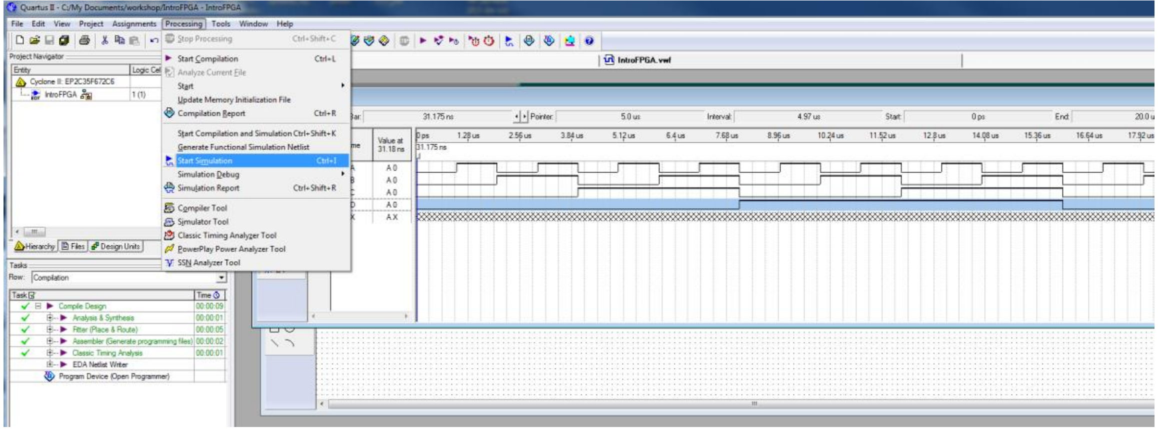
Save in: workshop

Name	Date modified	Type
db	6/13/2017 1:19 PM	File folder
incremental_db	6/13/2017 1:02 PM	File folder
IntroFPGA	6/13/2017 1:19 PM	Quartus II

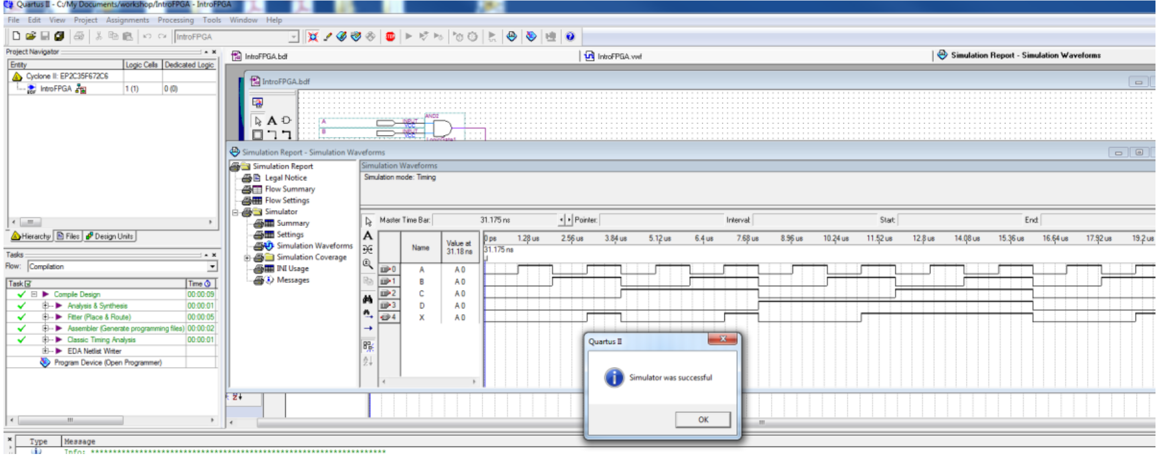
File name: IntroFPGA
Save as type: Vector Waveform File (*.vwf)
☑ Add file to current project
Save Cancel

E. Perform a simulation of the X-output

1) Choose Processing => Start Simulation


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation and Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
IntroFPGA.vwf

2) Show the results of the simulation for the Boolean equation X = AB+CD



Simulation mode: Timing

Master Time Bar: 31.175 ns

	Name	Value at 31.18 ns
0	A	A 0
1	B	A 0
2	C	A 0
3	D	A 0
4	X	A 0

Quartus II

Simulator was successful

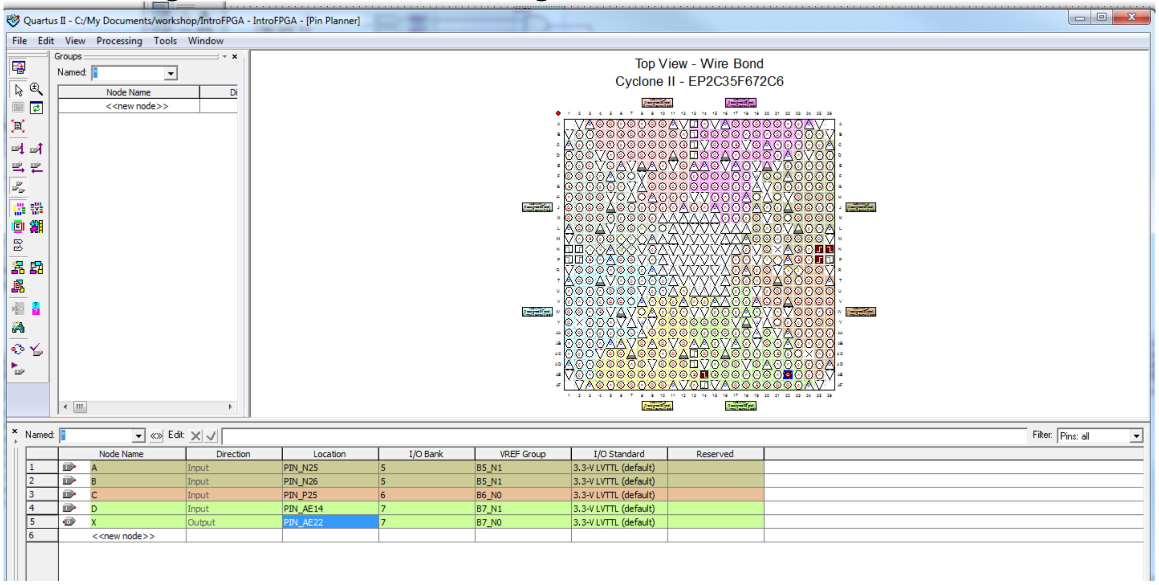
OK

F. Programming the FPGA using the Altera DE2 Programmer Board (hardware configuration)

1) Connect SW0, SW1, SW2, SW3 and LEDG0 to the associated pin number

Input Switch		Output LED Bank 1	
Switch Number	Pin Number	LED Number	Pin Number
SW0 (A)	PIN_N25	LEDG0 (X)	PIN_AE22
SW1 (B)	PIN_N26		
SW2 (C)	PIN_P25		
SW3 (D)	PIN_AE14		

2) Assign specific pin numbers in the IntroFPGA for connecting to the DE2 board Choose Assignment -> Pins from the assignment Editor screen

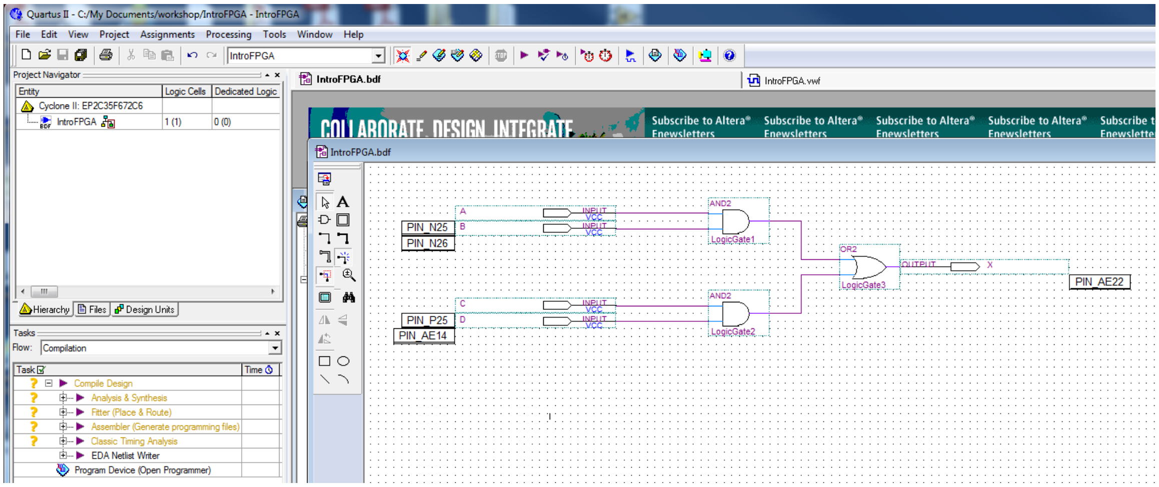


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA - [Pin Planner]
File Edit View Processing Tools Window
Groups
Named:
Node Name
<<new node>>
Top View - Wire Bond
Cyclone II - EP2C35F672C6
Named:
Edit:
Filter: Pins: all

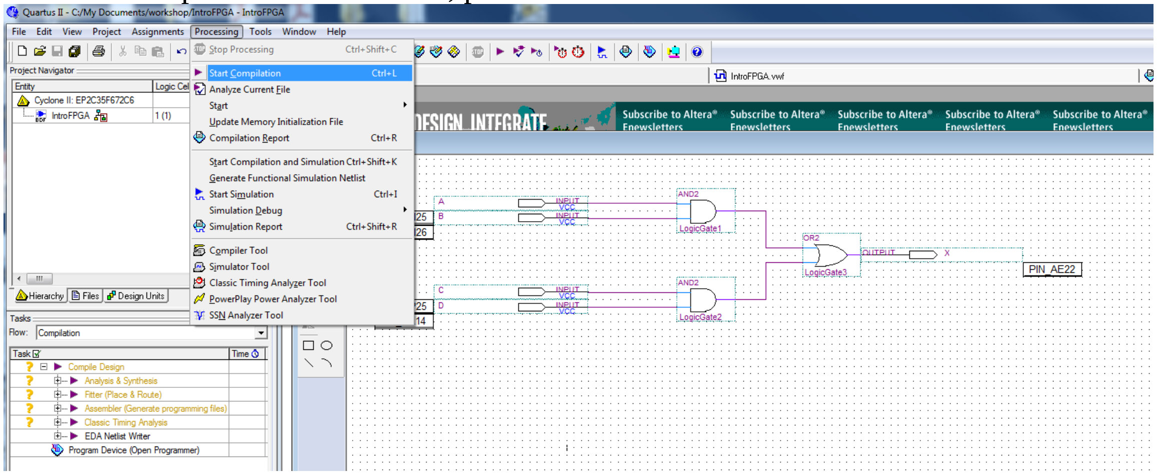
	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	A	Input	PIN_N25	5	B5_N1	3.3-V LVTTL (default)	
2	B	Input	PIN_N26	5	B5_N1	3.3-V LVTTL (default)	
3	C	Input	PIN_P25	6	B6_N0	3.3-V LVTTL (default)	
4	D	Input	PIN_AE14	7	B7_N1	3.3-V LVTTL (default)	
5	X	Output	PIN_AE22	7	B7_N0	3.3-V LVTTL (default)	
6	<<new node>>						

3) Choose File -> Save Project.

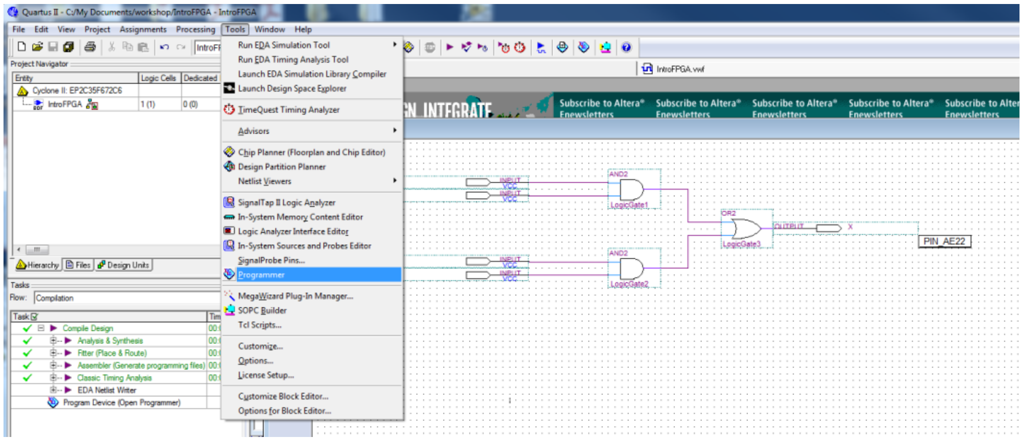
The bdf file showing the pin assignments



4) Choose Processing -> Compilation.
After the compilation is successful, press OK

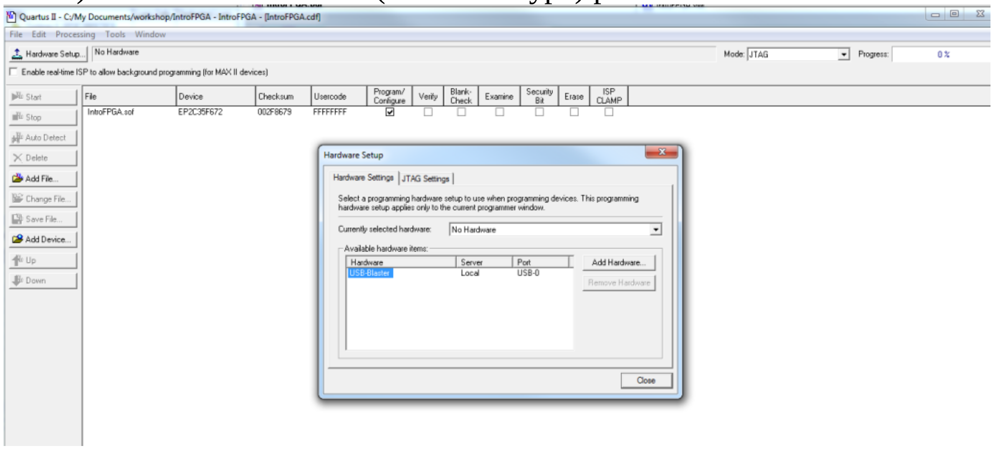

Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation and Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
IntroFPGA.vwf
PIN_AE22

5) JTAP Programing and Configuring the FPGA Device.The FPGA device must be programmed and configured to implement the designed circuit.
   i) Flip the RUN/PROG switch of DE2 development into the RUN position (default)
   ii) Choose Tools-> Programmer.


Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
Run EDA Simulation Tool
Run EDA Timing Analysis Tool
Launch EDA Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner (Floorplan and Chip Editor)
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
MegaWizard Plug-In Manager...
SOPC Builder
Tcl Scripts...
Customize...
Options...
License Setup...
Customize Block Editor...
Options for Block Editor...
IntroFPGA.vwf
PIN_AE22

iii) Click Hardware Setup -> Select Add Hardware

iv) Choose USB-Blaster (Hardware type) press Close



Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA - [IntroFPGA.cdf]

Hardware Setup... No Hardware — Mode: JTAG — Progress: 0 %

□ Enable real-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
IntroFPGA.sof	EP2C35F672	002F8679	FFFFFFFF	☑	□	□	□	□	□	□

Hardware Setup

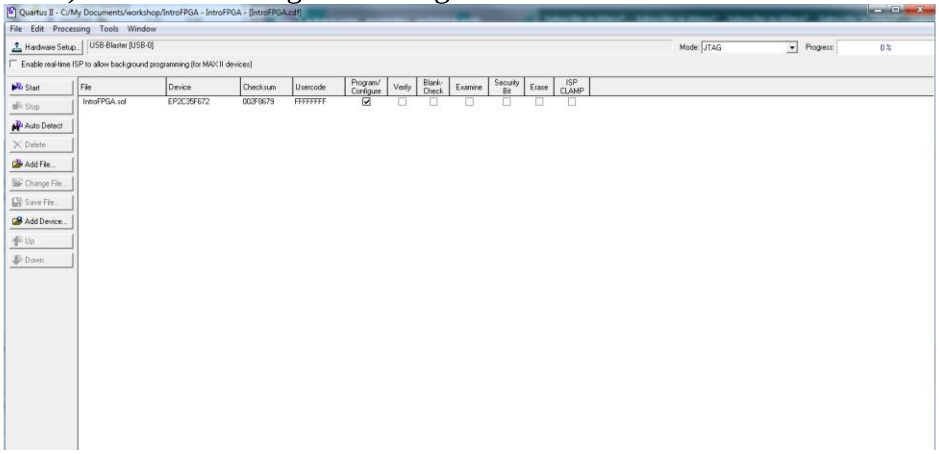
Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.

Currently selected hardware: No Hardware

Available hardware items:

Hardware	Server	Port
USB-Blaster	Local	USB-0

v) Make sure Program/Configure check box



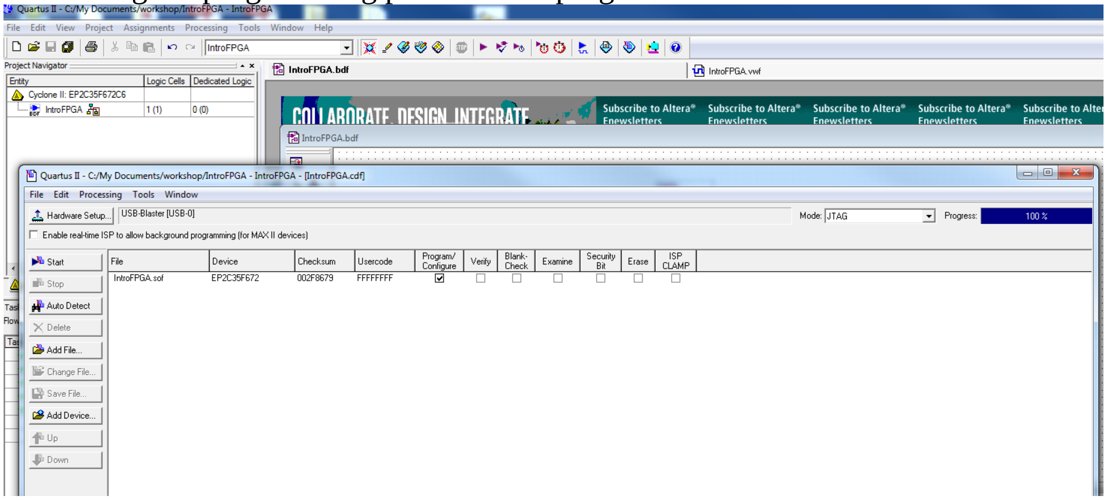
Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA - [IntroFPGA.cdf]

Hardware Setup... USB-Blaster [USB-0] — Mode: JTAG — Progress: 0 %

□ Enable real-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
IntroFPGA.sof	EP2C35F672	002F8679	FFFFFFFF	☑	□	□	□	□	□	□

6) Download the embedded system design to Altera EP2C35F672C6. Press Start for starting the programming process until progress 100%



Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA

Project Navigator

Entity	Logic Cells	Dedicated Logic
Cyclone II: EP2C35F672C6		
IntroFPGA	1 (1)	0 (0)

IntroFPGA.bdf — IntroFPGA.vwf

Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA - [IntroFPGA.cdf]

Hardware Setup... USB-Blaster [USB-0] — Mode: JTAG — Progress: 100 %

□ Enable real-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
IntroFPGA.sof	EP2C35F672	002F8679	FFFFFFFF	☑	□	□	□	□	□	□

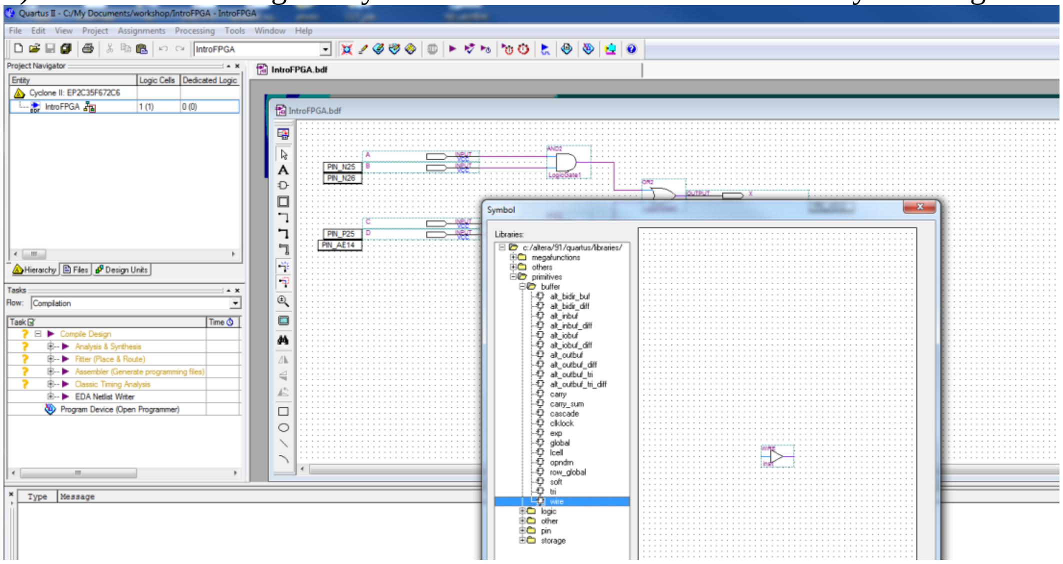
G. Test the download design (X = AB + CD) to the FPGA chip by combinations of input levels and observation of the output responds

Truth Table for Testing the FPGA program for X= AB+CD				
A (SW0)	B (SW1)	C (SW2)	D (SW3)	X(LED)
0 (DOWN)	0 (DOWN)	0 (DOWN)	0 (DOWN)	0 (Led off)
0 (DOWN)	0 (DOWN)	0 (DOWN)	1 (DOWN)	0 (Led off)
0 (DOWN)	0 (DOWN)	1 (UP)	0 (DOWN)	0 (Led off)
0 (DOWN)	0 (DOWN)	1 (UP)	1 (UP)	**1 (Led on)**
0 (DOWN)	1 (UP)	0 (DOWN)	0 (DOWN)	0 (Led off)
0 (DOWN)	1 (UP)	0 (DOWN)	1 (UP)	0 (Led off)
0 (DOWN)	1 (UP)	1 (UP)	0 (DOWN)	0 (Led off)
0 (DOWN)	1 (UP)	1 (UP)	1 (UP)	**1 (led on)**
1 (UP)	0 (DOWN)	0 (DOWN)	0 (DOWN)	0 (Led off)
1(UP)	0 (DOWN)	0 (DOWN)	1 (UP)	0 (Led off)
1 (UP)	0 (DOWN)	1 (UP)	0 (DOWN)	0 (Led off)
1 (UP)	0 (DOWN)	1 (UP)	1 (UP)	**1 (Led on)**
1 (UP)	1 (UP)	0 (DOWN)	0 (DOWN)	**1 (Led on)**
1 (UP)	1 (UP)	0 (DOWN)	1 (UP)	**1 (Led on)**
1 (UP)	1 (UP)	1 (UP)	0 (DOWN)	**1 (Led on)**
1 (UP)	1 (UP)	1 (UP)	1 (UP)	**1 (Led on)**

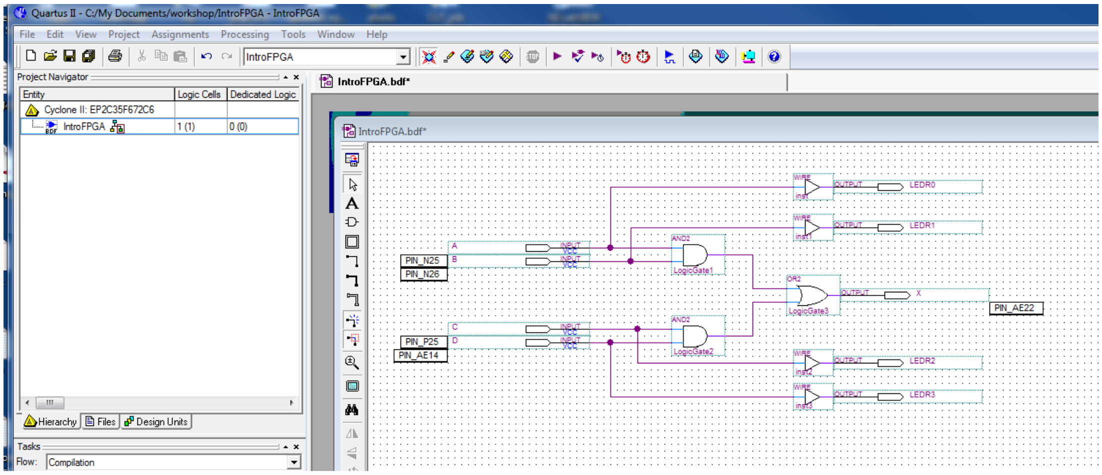
H. Your turn – Practice

Follow the steps to update your design by adding four buffers. Design and test the logic to implement the circuit shown in the figure bellow.

1) Work on the design entry IntroFPGA.bdf and insert buffers to your design

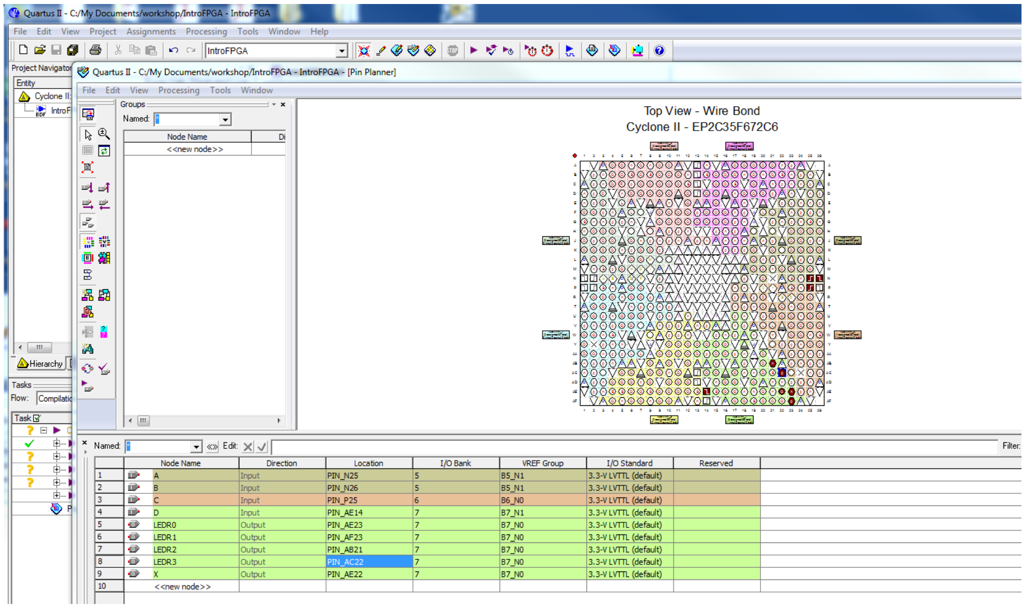


2) Insert output pins and update the names of outputs: LEDR0, LEDR1, LEDR2, and LEDR3



3) Save your file and Compile your design and see if any error

4) Update Pin Planner and configuration to make connection between logic pins to associated FPGA pins.

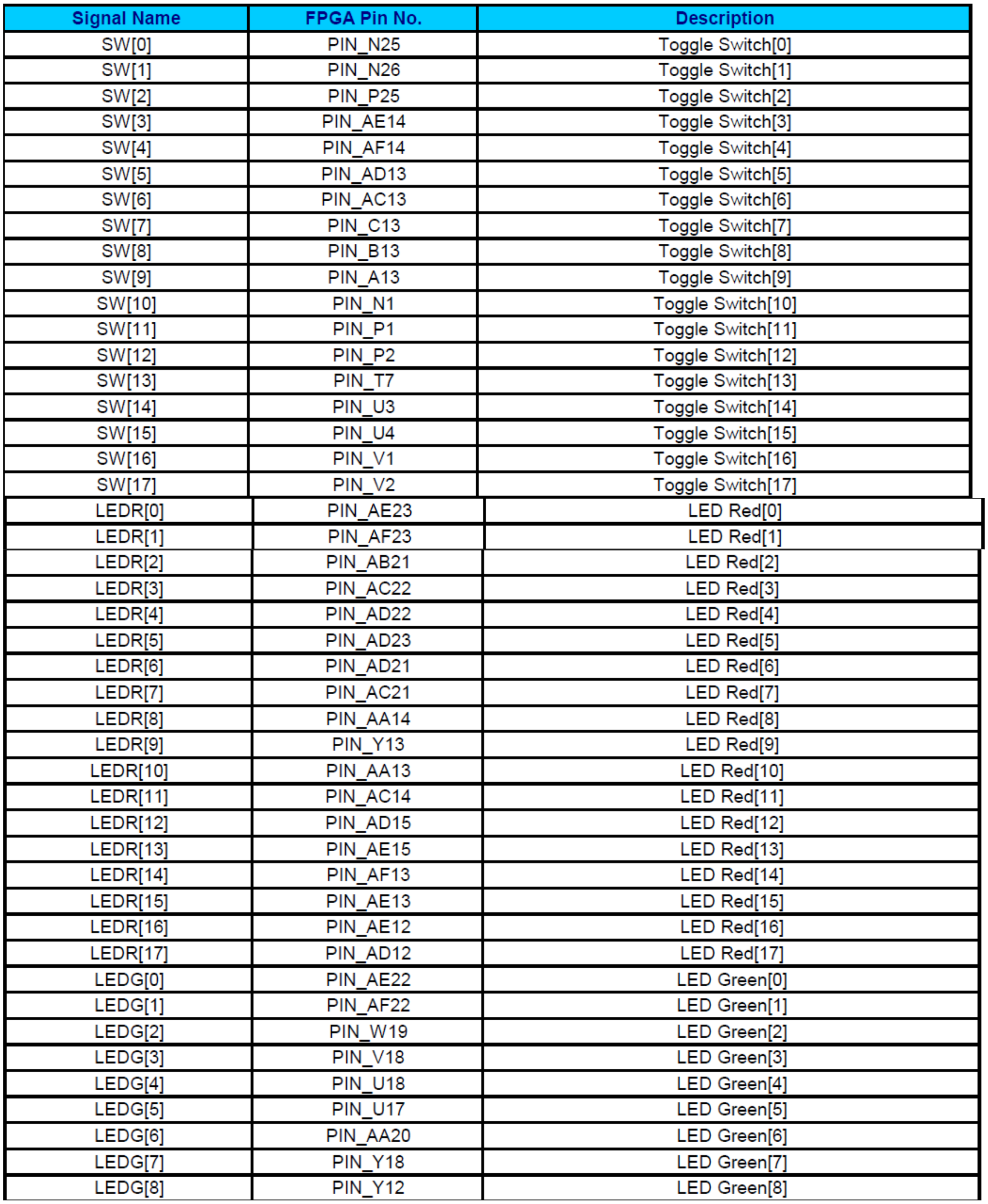

Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA
File Edit View Project Assignments Processing Tools Window Help
IntroFPGA
Quartus II - C:/My Documents/workshop/IntroFPGA - IntroFPGA - [Pin Planner]
File Edit View Processing Tools Window
Groups
Named:
Node Name
<<new node>>
Top View - Wire Bond
Cyclone II - EP2C35F672C6
Named:
Edit:
Filter:

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	A	Input	PIN_N25	5	B5_N1	3.3-V LVTTL (default)	
2	B	Input	PIN_N26	5	B5_N1	3.3-V LVTTL (default)	
3	C	Input	PIN_P25	6	B6_N0	3.3-V LVTTL (default)	
4	D	Input	PIN_AE14	7	B7_N1	3.3-V LVTTL (default)	
5	LEDR0	Output	PIN_AE23	7	B7_N0	3.3-V LVTTL (default)	
6	LEDR1	Output	PIN_AF23	7	B7_N0	3.3-V LVTTL (default)	
7	LEDR2	Output	PIN_AB21	7	B7_N0	3.3-V LVTTL (default)	
8	LEDR3	Output	PIN_AC22	7	B7_N0	3.3-V LVTTL (default)	
9	X	Output	PIN_AE22	7	B7_N0	3.3-V LVTTL (default)	
10	<<new node>>						

5) Compile your design with FPGA device hardware

6) Download the design to FPGA IC. Observe the output LEDs and inputs Switches

7) Explore different led lights by your own.



Signal Name	FPGA Pin No.	Description
SW[0]	PIN_N25	Toggle Switch[0]
SW[1]	PIN_N26	Toggle Switch[1]
SW[2]	PIN_P25	Toggle Switch[2]
SW[3]	PIN_AE14	Toggle Switch[3]
SW[4]	PIN_AF14	Toggle Switch[4]
SW[5]	PIN_AD13	Toggle Switch[5]
SW[6]	PIN_AC13	Toggle Switch[6]
SW[7]	PIN_C13	Toggle Switch[7]
SW[8]	PIN_B13	Toggle Switch[8]
SW[9]	PIN_A13	Toggle Switch[9]
SW[10]	PIN_N1	Toggle Switch[10]
SW[11]	PIN_P1	Toggle Switch[11]
SW[12]	PIN_P2	Toggle Switch[12]
SW[13]	PIN_T7	Toggle Switch[13]
SW[14]	PIN_U3	Toggle Switch[14]
SW[15]	PIN_U4	Toggle Switch[15]
SW[16]	PIN_V1	Toggle Switch[16]
SW[17]	PIN_V2	Toggle Switch[17]
LEDR[0]	PIN_AE23	LED Red[0]
LEDR[1]	PIN_AF23	LED Red[1]
LEDR[2]	PIN_AB21	LED Red[2]
LEDR[3]	PIN_AC22	LED Red[3]
LEDR[4]	PIN_AD22	LED Red[4]
LEDR[5]	PIN_AD23	LED Red[5]
LEDR[6]	PIN_AD21	LED Red[6]
LEDR[7]	PIN_AC21	LED Red[7]
LEDR[8]	PIN_AA14	LED Red[8]
LEDR[9]	PIN_Y13	LED Red[9]
LEDR[10]	PIN_AA13	LED Red[10]
LEDR[11]	PIN_AC14	LED Red[11]
LEDR[12]	PIN_AD15	LED Red[12]
LEDR[13]	PIN_AE15	LED Red[13]
LEDR[14]	PIN_AF13	LED Red[14]
LEDR[15]	PIN_AE13	LED Red[15]
LEDR[16]	PIN_AE12	LED Red[16]
LEDR[17]	PIN_AD12	LED Red[17]
LEDG[0]	PIN_AE22	LED Green[0]
LEDG[1]	PIN_AF22	LED Green[1]
LEDG[2]	PIN_W19	LED Green[2]
LEDG[3]	PIN_V18	LED Green[3]
LEDG[4]	PIN_U18	LED Green[4]
LEDG[5]	PIN_U17	LED Green[5]
LEDG[6]	PIN_AA20	LED Green[6]
LEDG[7]	PIN_Y18	LED Green[7]
LEDG[8]	PIN_Y12	LED Green[8]