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Non-Volatile Storage- (SCM)

 DRAM (Dynamic Random Access Memory) is a type of memory that has been a favorite for years to write data to disks, such as in laptop hard drives. The next thing to watch is called SCM (Storage Class memory), this next storage system technology has gained a lot of traction in the tech world. Currently HP & SanDisk entered a long term alliance to explore enterprise SCM products such as servers, also Intel Micro, IBM Samsung and about 2 dozen companies are working on phase changing memory. Storage Class Memory is a type of memory that could possibly replace DRAM, and supplement NAND flash as a higher class memory. When put next to HDD’s mechanics; SCM could offer a near limitless capacity in comparison. The problem with hard drives is that in many cases they are unable to provide information to the application quickly enough.

You may ask why is this so important to the technology industry? One reason is that when building large systems, there has always been a latency gap between CPU and Disk, memory like DRAM travels in the nanoseconds, whereas storage memory such as reading and writing is usually measured in milliseconds. This has been a problem for a long time but there were too many issues when trying to close this latency gap, SCM is hopeful that they will succeed where many others have fell short; to utilize its resources effectively to close this gap, but that’s easier said than done. Some features of SCM are: it will be a Solid State Drive (no moving parts), short access times (within the DRAM range), Low cost per bit (disk like prices), and its non-volatility. If they can deliver half of what they expect, SCM will position itself in the place to revolutionize the way in which we handle large servers and their information.

 DRAM memory is volatile, which means that there needs to be an active power connection to function. The advantages of volatile memory are: it functions fast, and it is well-suited to protecting sensitive information. A disadvantage is when the power to a volatile memory source is shut off, volatile memory loses its contents, and the information is subsequently deleted. SCM is persistent, meaning that information is not lost when, or if the server crashes or loses power. Another shortcoming with hard drives is that in many cases they are unable to provide information to the application quickly enough. Storage class memory is being created out of flash-based NAND that can provide an intermediate level between high performance DRAM and cost effective HDD’s. Replacing volatile memory with fast non-volatile memory will have an enormous impact on the performance and efficiency of microprocessor based systems. In addition to that SCM is expected to offer significant cost benefits, faster I/O rates, and persistence improvements over conventional technologies such as DRAM.

SCM has significant improvements of DRAM there are some other constraints that can hinder its optimal performance, such as bottlenecking from legacy connectivity’s, or be required to process unusually high levels of application threading. Another performance problem that has been theorized is garbage collection, the process of preparing old flash cells to receive new data. If this garbage collection occurs during inbound write cycles, the added overhead could significantly reduce write performance. Also, because each controller only has the flash it’s been assigned, other flash on the board won’t be available to replace the bad cells that accumulate over time. Down the line this may leave one controller with an inadequate amount of flash memory while other controllers have plenty of cells.

Storage Class Memory fills a latency gap which has been a problem since we started writing information to disks, while also promising to benefit all aspects of how we handle datacenters non-volatile storage memory, especially in regards to enterprise servers and big data centers. Despite all the pro’s and con’s this could open the door to new architectures in which information doesn’t have to be shuffled from slow storage devices to faster memory locations to be properly utilized. These architectures would be capable of taking huge amounts of data and crunching them far more efficiently than existing machines have the capacity to perform.

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