Magnitude Comparator Circuit

Experiment 9

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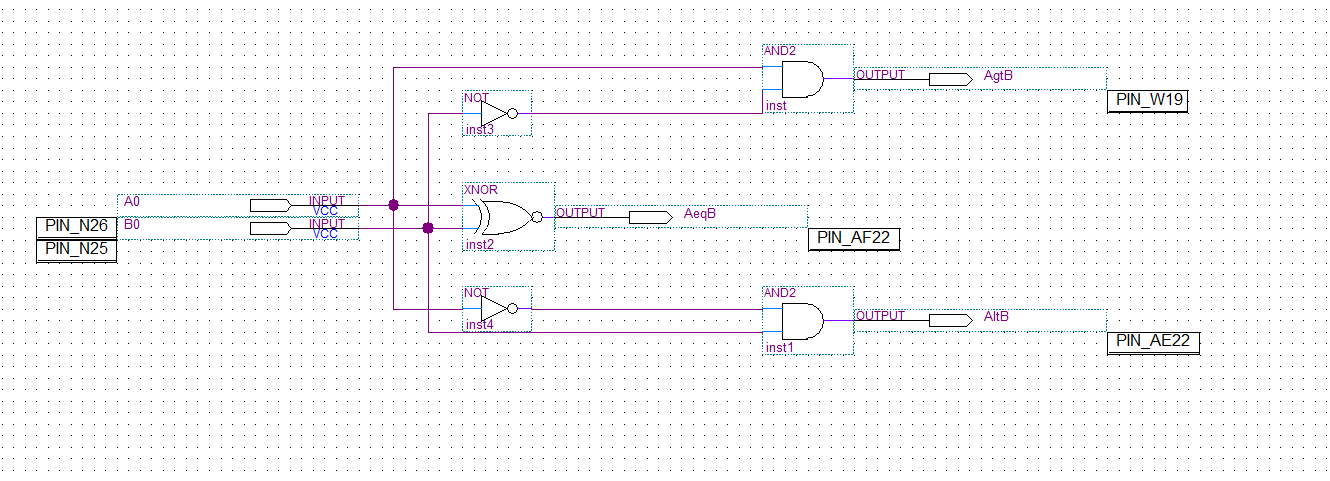
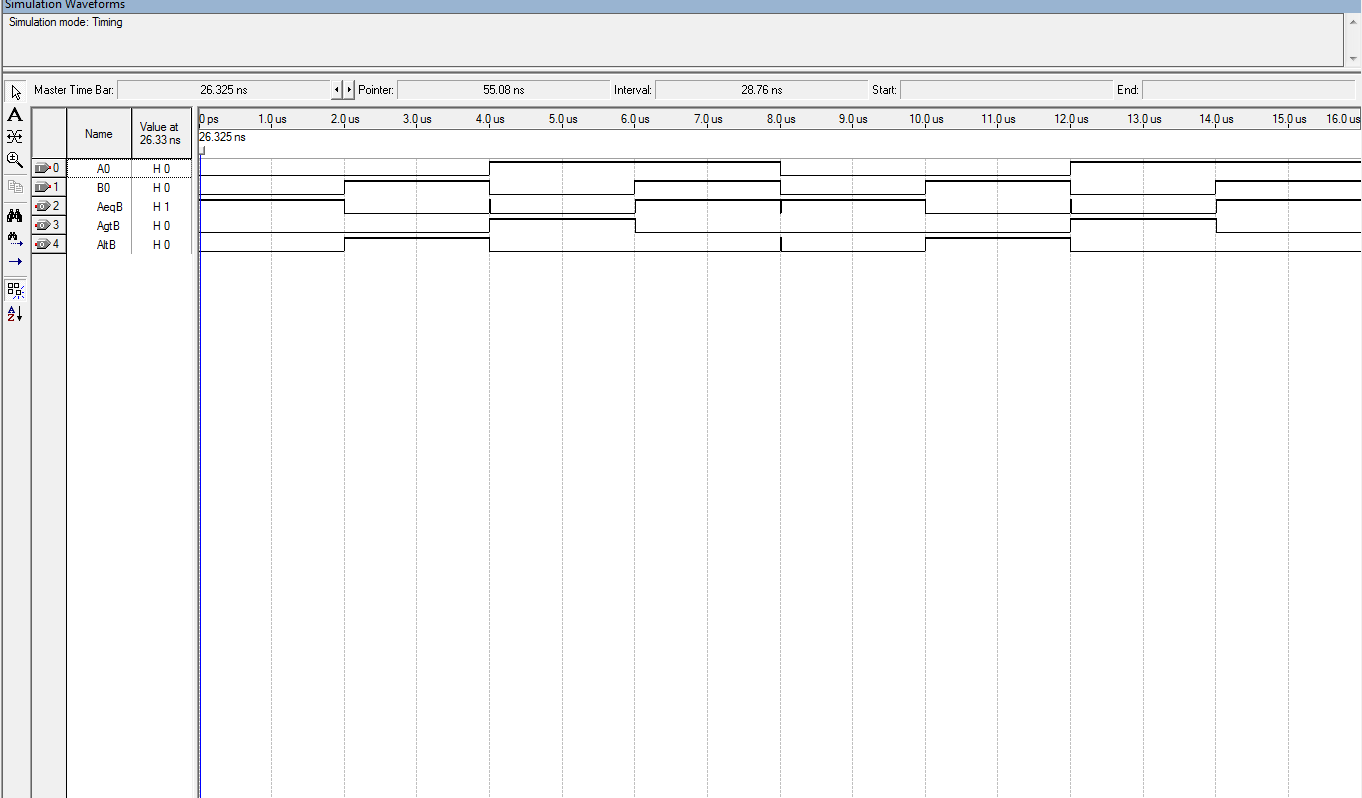
Objective

* To build 1-bit and 2-bit Magnitude Comparator circuits using the Quartus 2 development software with the DE-2 board.
* To test the design by downloading the file into the DE-2 board, exercising the inputs with toggle switches and observing 3 individual LED’s

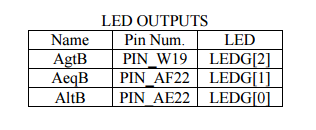
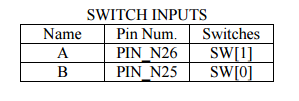
Materials

* Quartus IIR Web Edition V9.1 SP2 software by Altera Corporation
* Altera DE2 FPGA board
* USB Drive

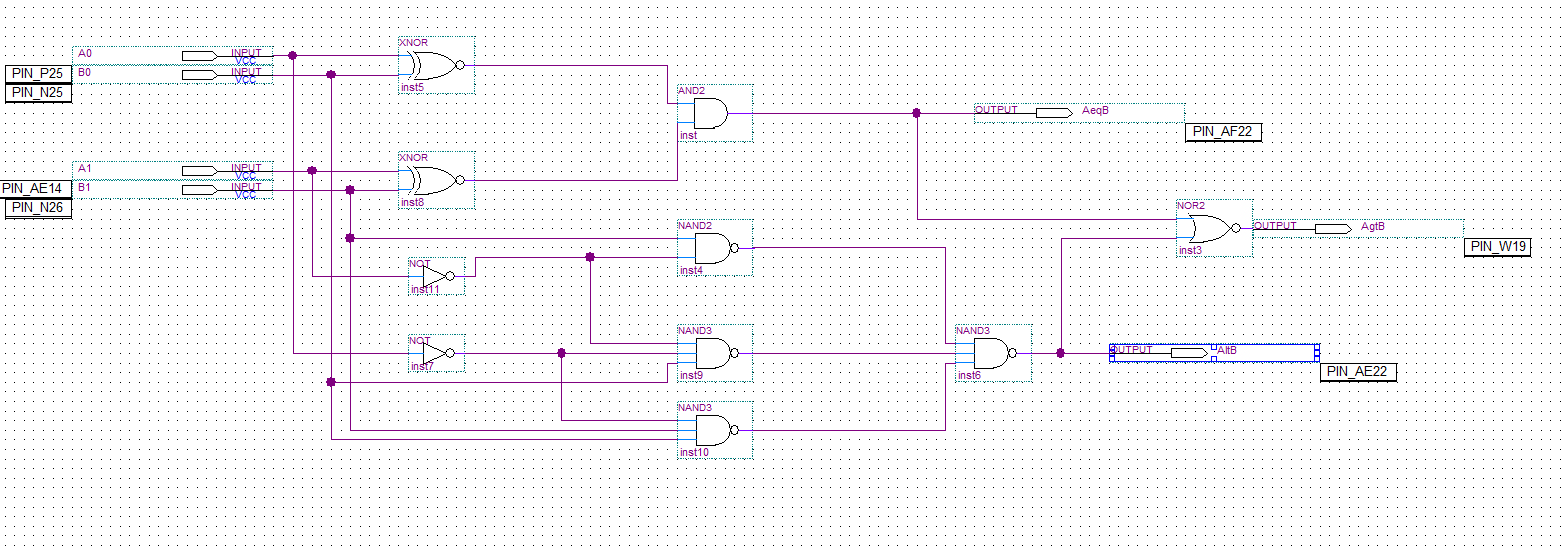
Part 1:

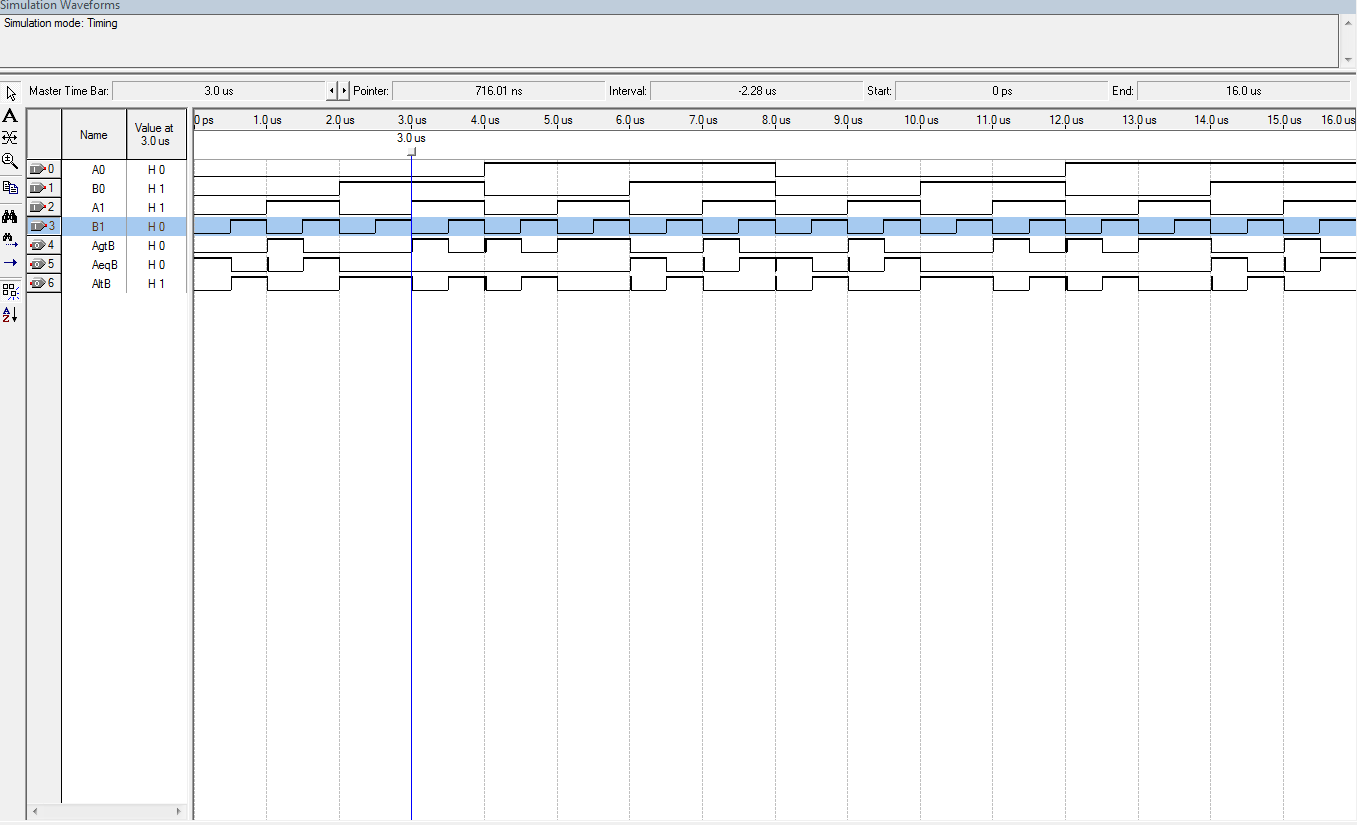


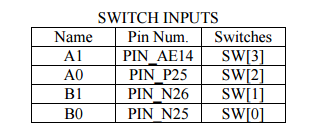
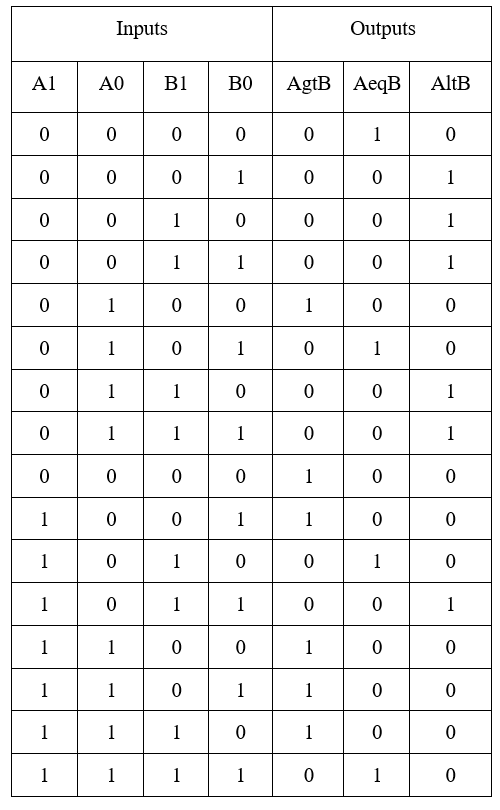
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs | | Outputs | | |
| A0 | B0 | Agtb | Aeqb | Altb |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |



Part 2:







Conclusion

In this laboratory exercise we learned how to develop 1 bit and 2 bit Magnitude comparators using Quartus II software and were able to upload these designs into an Altera-DE2 board.