7-Segment Display with VDML

Experiment 8

Michael Robayo, Galib Rahman

04/24/2017

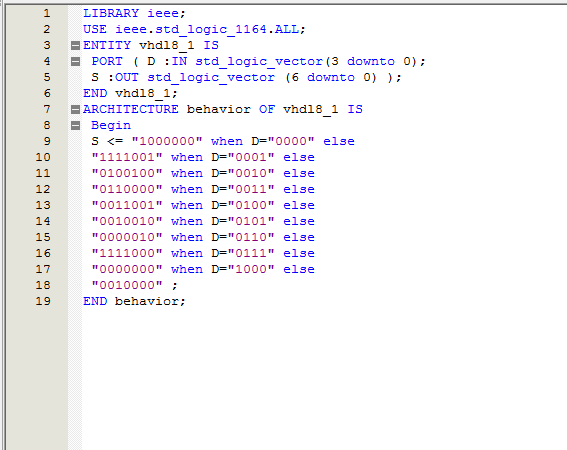
Objective

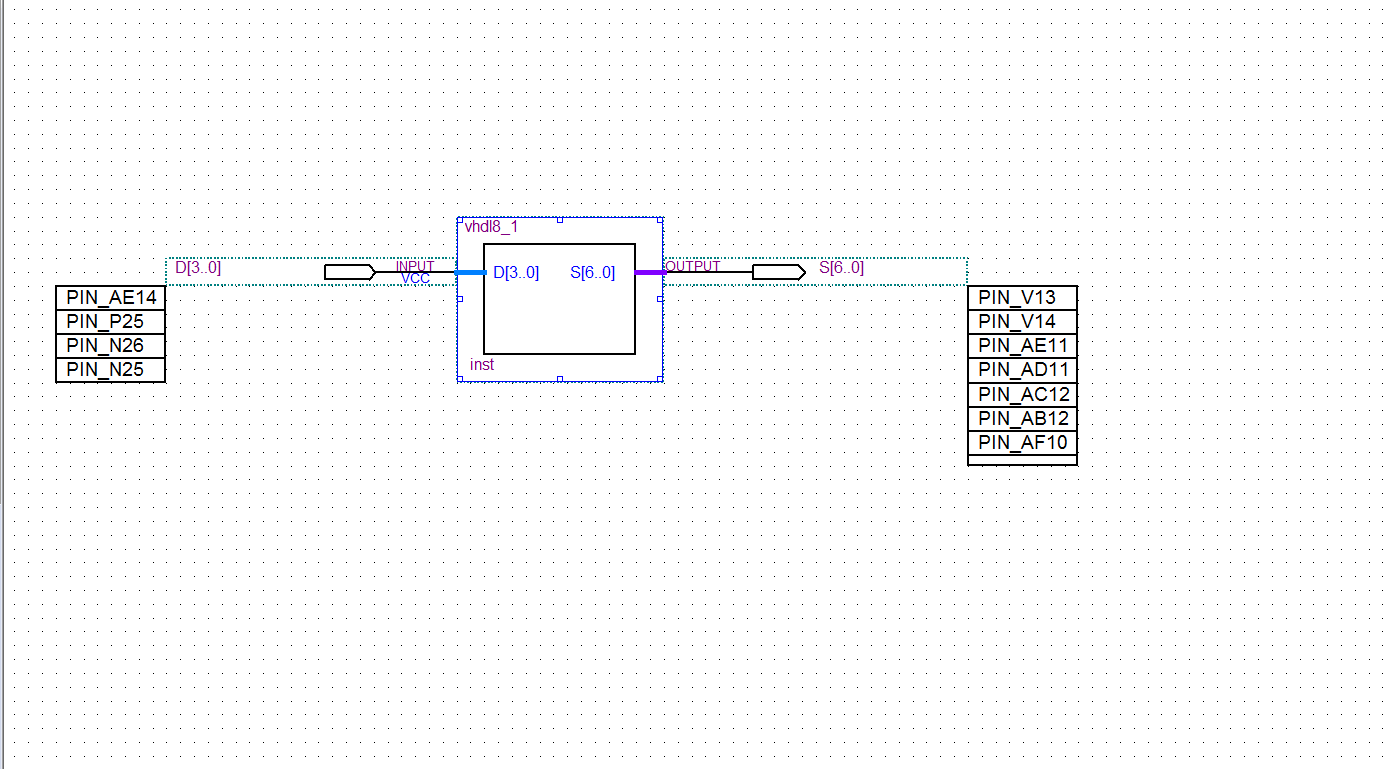
* Use simple VHDL assignment statements to represent a function table
* Introduce the selected signal assignments WHEN-ELSE clause
* Display hexadecimal numbers (0 through F) on the 7-segment LED of the DE-2 board

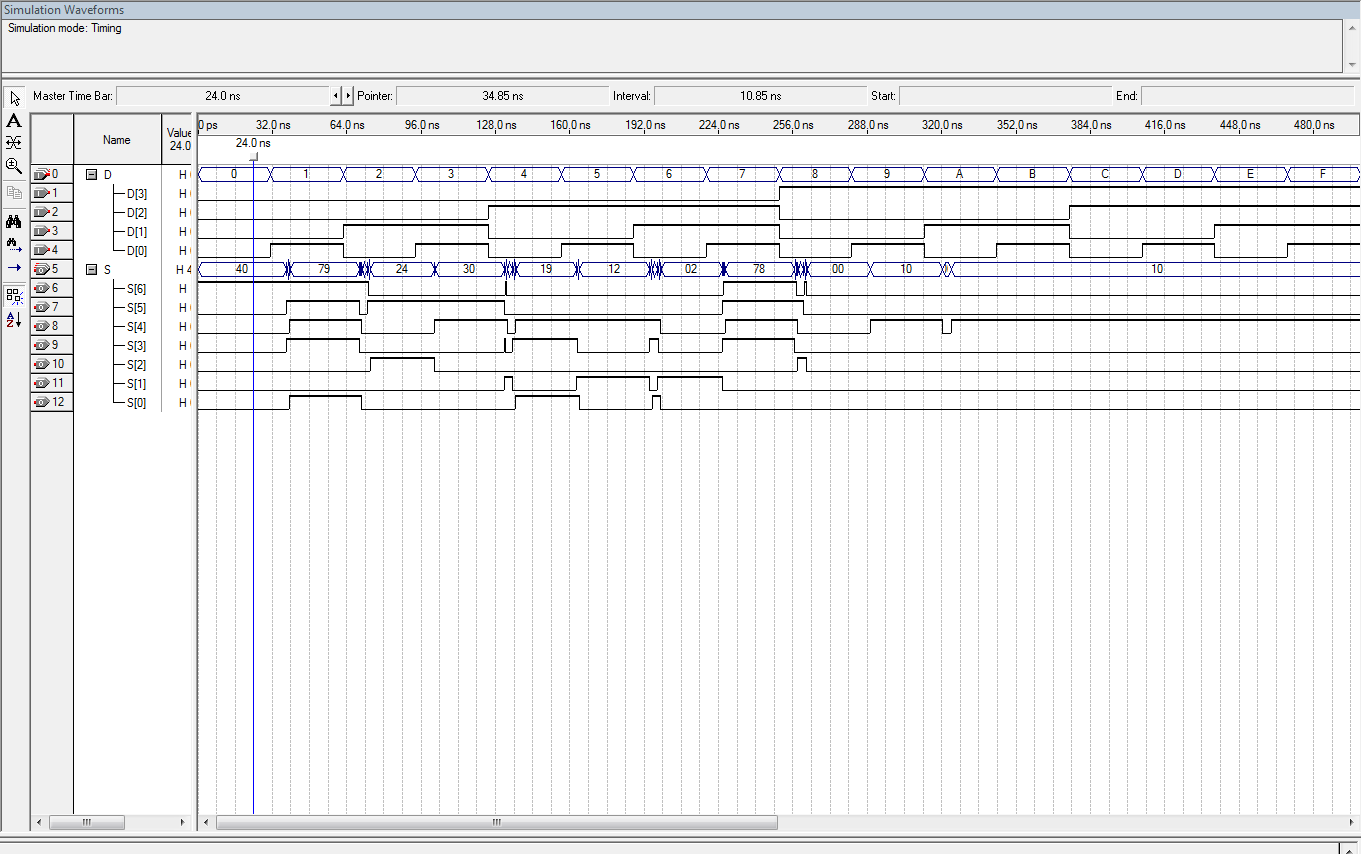
Materials

* Quartus IIR Web Edition V9.1 SP2 software by Altera Corporation
* Altera DE2 FPGA board
* USB Drive

Part 01

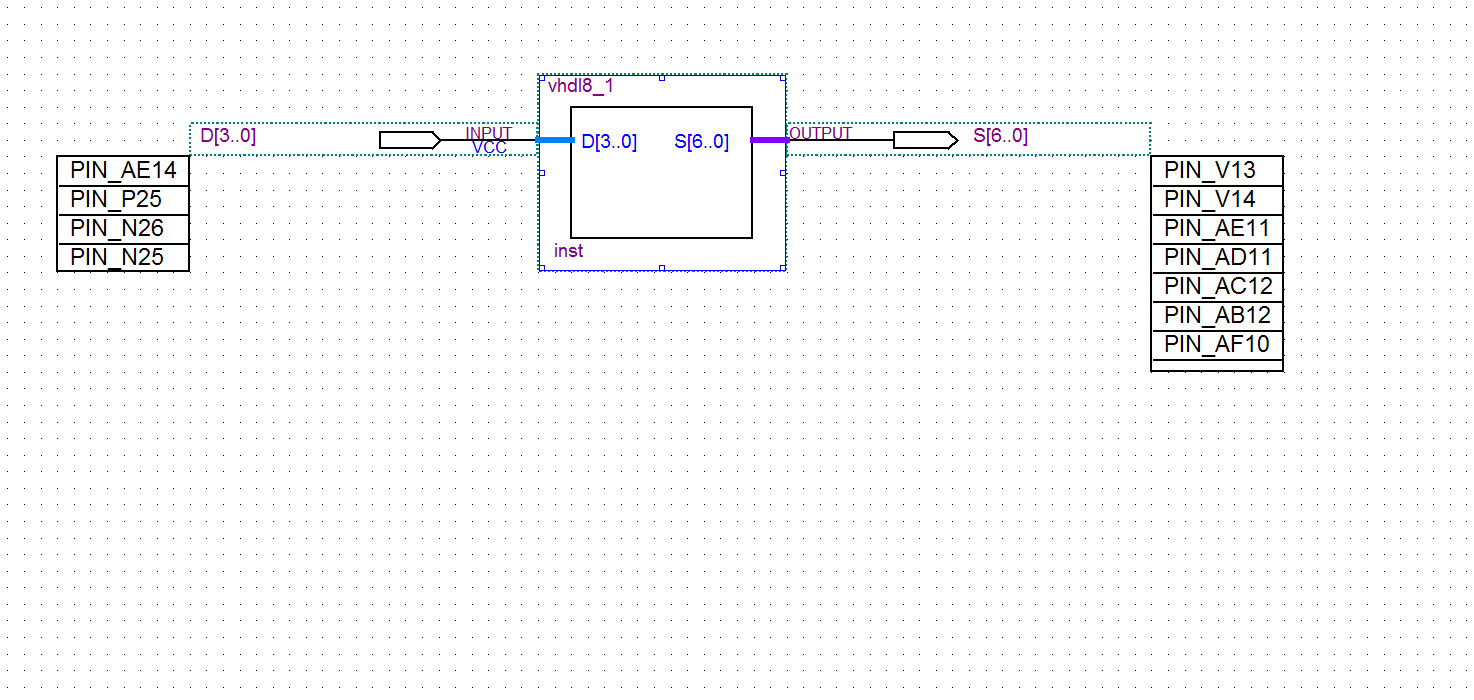


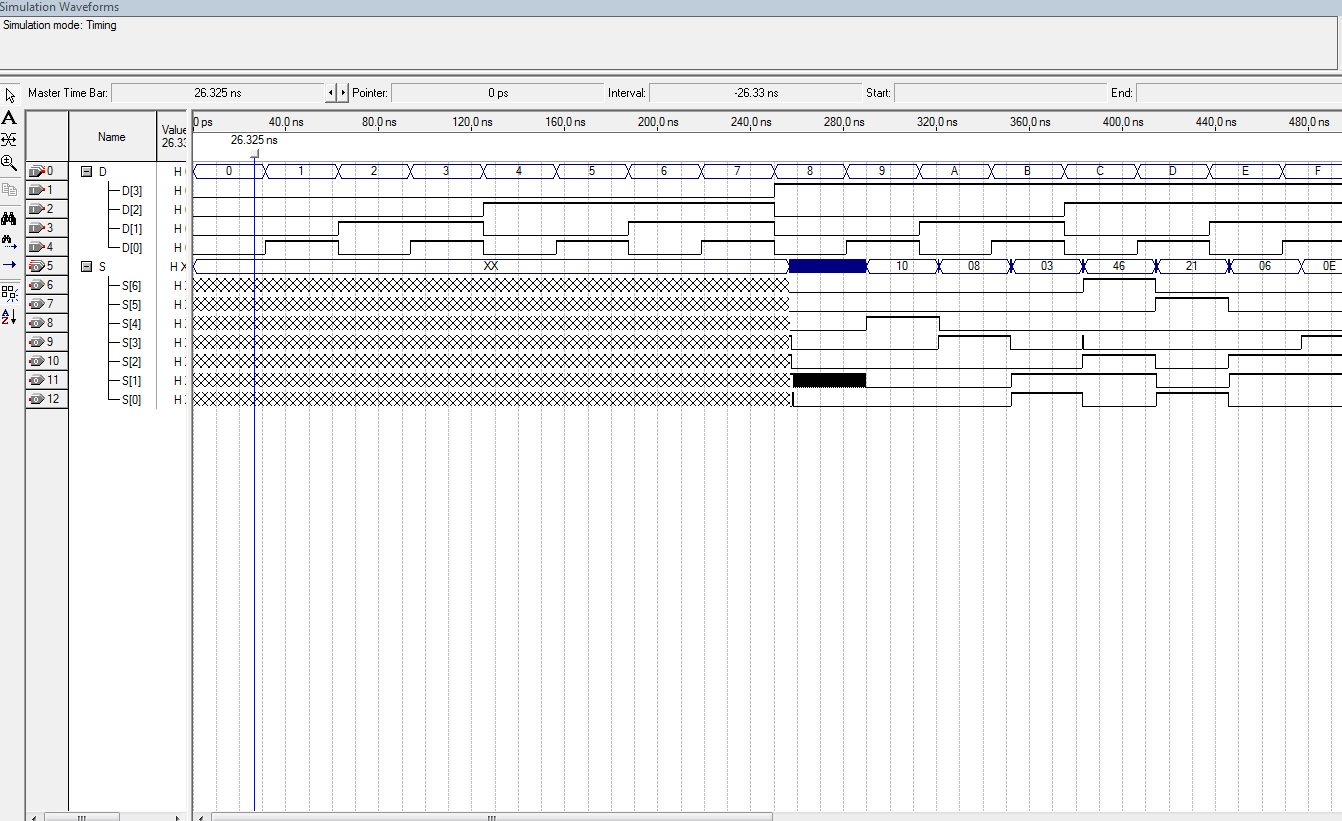




Part 02







Conclusion

In this laboratory exercise we were able to use simple VHDL assignment statements to represent a function table,introduce the selected signal assignments WHEN-ELSE clause and display hexadecimal numbers (0 through F) on the 7-segment LED of the DE-2 board.