Introduction to D and J-K Flip-Flop

Experiment 11

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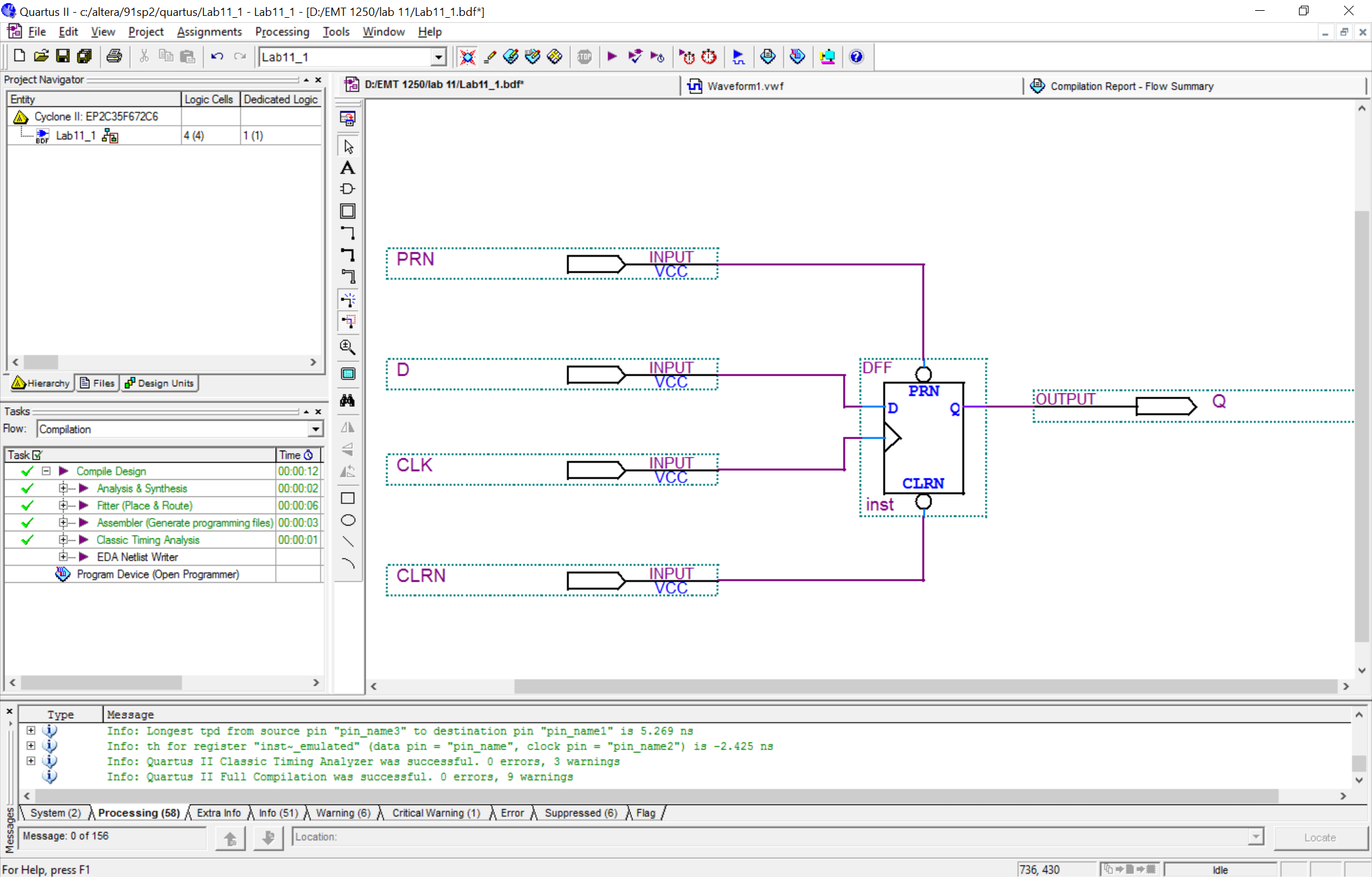
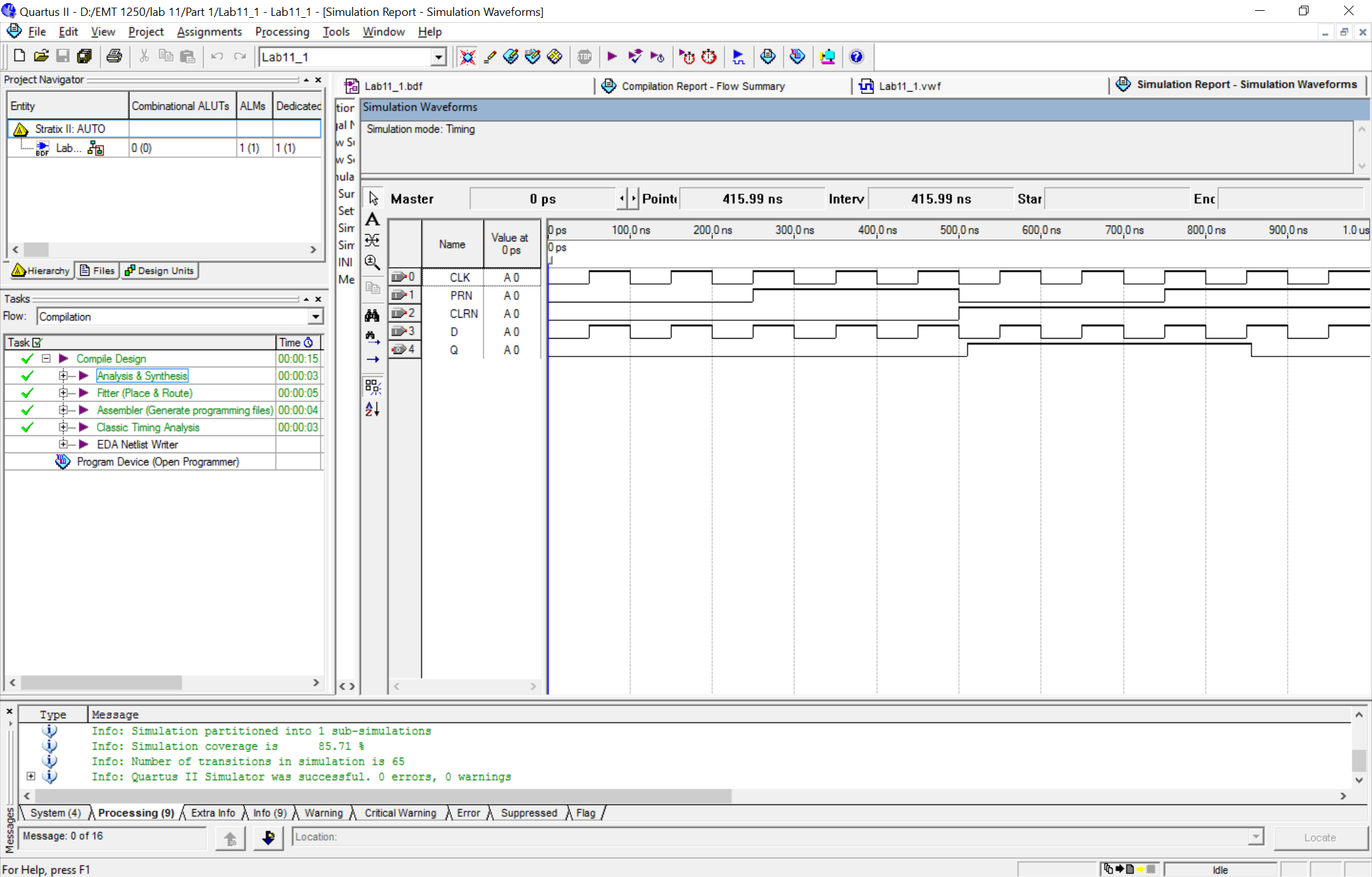
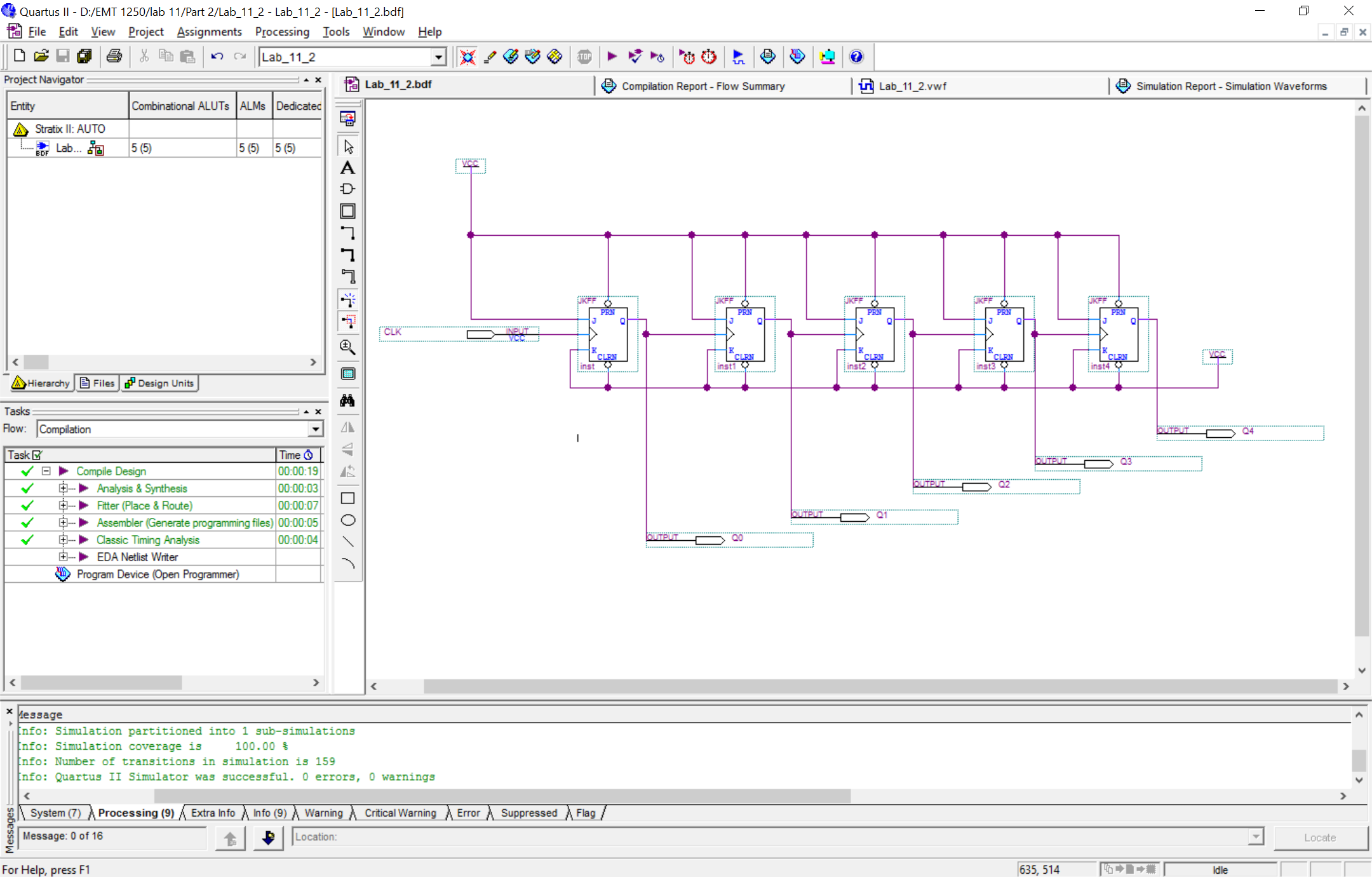
Objective

* To investigate the behavior of a D flip flop with the Altera Quartus II program. A simulation waveform will be constructed and used to exercise the inputs and observe the resulting output.
* To show how flip flops can be used as frequency dividers/counters. The DE-2 board will be programmed with JK flip flops configured as a frequency divider/counter.

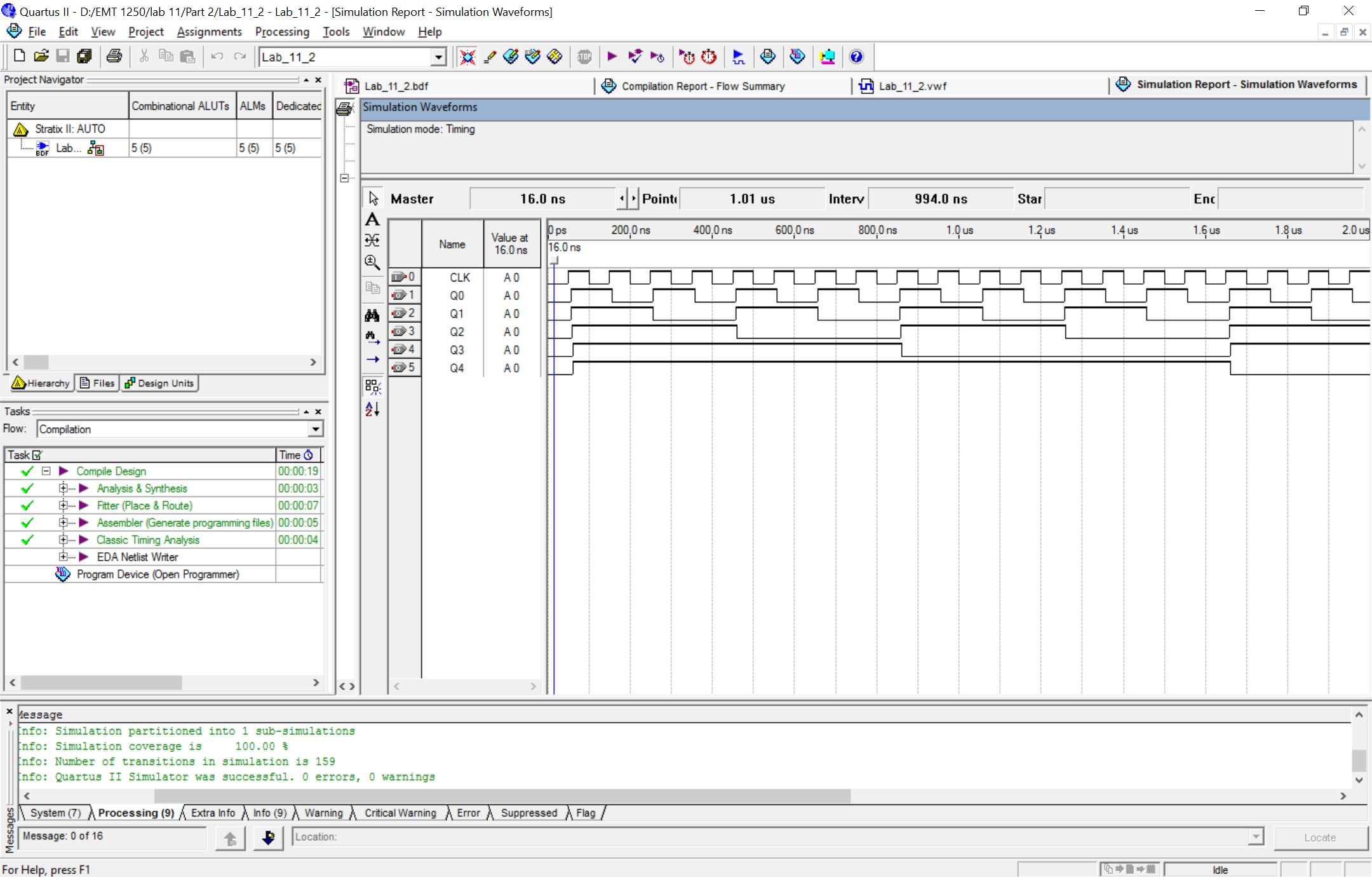
Materials

* PC (Altera Quartus II V9.1 installed)
* DE-2 board

Part 1



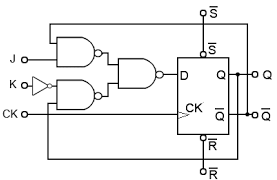
Part 2



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q0 | Q1 | Q2 | Q3 | Q4 |
| tc0=5.8 ns | tc0=7.129 ns | tc0=9.974 ns | tc0=11.191 ns | tc0=12.252 ns |

Questions

1. A JK flip flop can be made to operate as a D flip flop by adding an external Inverter gate and making the appropriate connections. Draw the schematic for this circuit.



2. A D flip flop can be made to operate in a toggle mode (divide its CLOCK input frequency by two) by adding an external Inverter gate and making the appropriate connections. Draw the schematic for this circuit.

3. Circuitry in a digital clock takes the output of a 65,536 Hz Oscillator and divides it down to 1 Hz (1 pulse per second). How many flip flops are needed to do this?

6 Flip Flops

4. Write in the states (Reset, Set, Asynch. Reset, Asynch. Set) on the output waveforms of the D flip flop from Part 1.

Conclusion

In this laboratory exercise we observed the behavior of the D flip flop using Quartus II software, and programmed the Altera DE-2 Board with JK flip flops in configuration of a frequency divider/counter. In part 2, we encountered some issues in creating an Up counter, by following the procedure directly. Via experimentation we realized that the Altera DE-2 Board provided an inverted version of what we wished to program, thus to create an UP counter we added inverters to every output as shown below :

