NAND & NOR Gates

Experiment 3

Michael Robayo, Galib Rahman

02/22/17

Objective:

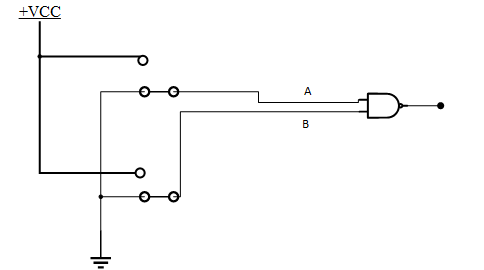
* To investigate the operation of the **NAND** and **NOR** Gates.
* To form other basic gates using the **NAND** and **NOR** Gates.

Materials:

* 5V DC Power Supply
* Digital Trainer (Logic Probe)
* Breadboard
* DIP Switch
* 7400 (NAND gate)
* 7402 (NOR gate)

Schematic Diagrams

NAND GATE: 1



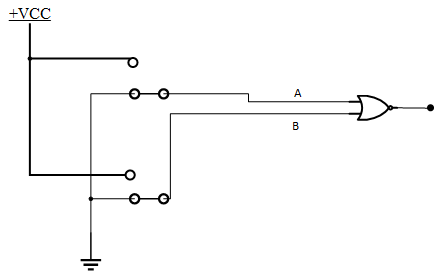
NAND GATE:2



NAND GATE:3



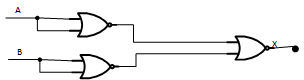
NOR GATE:1



NOR GATE:2

X

NOR GATE:3



Data:

**The NAND Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| A | **B** | **X** | **Volts Measured** |
| **0** | **0** | **1** | **5.03 V** |
| **0** | **1** | **1** | **5.03 V** |
| **1** | **0** | **1** | **5.03 V** |
| **1** | **1** | **0** | **0 V** |

**The NAND Gate with Inputs Connected Together**

|  |  |  |
| --- | --- | --- |
| **A** | **X** | **Volts Measured** |
| **0** | **1** | **5.03 V** |
| **1** | **0** | **0 V** |

**NAND Gates in Series with Inputs Connected Together**

|  |  |  |
| --- | --- | --- |
| **A** | **X** | **Volts Measured** |
| **0** | **0** | **0 V** |
| **1** | **1** | **3.58 V** |

**The NOR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| A | **B** | **X** | **Volts Measured** |
| **0** | **0** | **1** | **5.03 V** |
| **0** | **1** | **0** | **0 V** |
| **1** | **0** | **0** | **0 V** |
| **1** | **1** | **0** | **0 V** |

**The NOR Gate with Inputs Connected Together**

|  |  |  |
| --- | --- | --- |
| **A** | **X** | **Volts Measured** |
| **0** | **1** | **3.50 V** |
| **1** | **0** | **0 V** |

**Three NOR Gates Connected; Two NOR Gates each with Inputs Connected together serving as inputs for one NOR Gate**

|  |  |  |  |
| --- | --- | --- | --- |
| A | **B** | **X** | **Volts Measured** |
| **0** | **0** | **0** | **0 V** |
| **0** | **1** | **0** | **0 V** |
| **1** | **0** | **0** | **0 V** |
| **1** | **1** | **1** | **3.50 V** |

Questions and answers:

1. \_\_ \_\_\_\_What are the Boolean expressions for the NAND and NOR gates?

NAND: X=AB NOR: X=A+B

1. How does a NAND gate differ from an AND gate?

A NAND gate is the opposite of an AND Gate having included an inverter

1. How does a NOR gate differ from an OR gate?

A NOR gate is the opposite of an OR gate having inverted outputs compared to the output of an OR gate.

1. Under what input conditions is the output of a 2 input NOR gate LOW? Under what input conditions is the output of a 2 input NAND gate HIGH?

NOR gate: whenever any of the inputs are a HIGH there will be a LOW output.

NAND gate: whenever any input is a LOW the output will be a HIGH.

1. From the data in the experiment, how can you configure a NAND or NOR gate to function like an inverter?

In order to configure a NAND or NOR gate to function like an inverter, assuming it has two inputs, you combine the two inputs to function as an inverter.

Conclusion:

In Conclusion, in this experiment we learned how to manipulate NAND and NOR gates in order to gain outputs we would desires using our knowledge of logic gates. An AND gate would only have a HIGH output it must have all Inputs as HIGH. Since a NAND gate is the exact opposite of AND gate meaning that, whenever there is a LOW input the output will be HIGH and when all inputs are HIGH the output will be LOW. NOR gate is also the exact opposite of an OR gate. An OR gate has a HIGH output whenever there is at least one LOW Input; therefore, a NOR gate is the exact opposite meaning whenever there is at least one HIGH input there will be a LOW output. One thing we learned during this experiment was the manipulation of a NAND and NOR gate in order to act as an inverter. To do this, by combining the inputs together making it to have only one input, the Gate itself will act as an inverter by changing a LOW input to a HIGH input or vise versa.