Basic Logic Gates

Experiment 2

Michael Robayo, Galib Rahman

1/14/17

Objective:

* To exam a logic circuit and investigate the operation of the NOT, OR and AND gates.
* To verify logic truth tables from the voltages measured.

Materials:

* 5V DC power Supply
* Digital trainer (logic probe)
* Breadboard
* DIP Switch
* 7404 (inverter)
* 7408 (AND gate)
* 7432 (OR gate)
* Digital Multimeter

Schematic Diagram:







Data:

The NOT Gate



The OR Gate



The AND Gate

Questions and answers:

**1.What are the Boolean expressions for the NOT, OR, and AND gates?**

*Let, A & B represent the two inputs and x represent the output, the boolean expressions for each gate may be represented as follows:*

*OR Gate may be represented by the boolean expression x=A+B*

*AND Gate may be represented by the boolean expression x=AB*

*NOT Gate may be represented by the boolean expression x=Ā*

 **2. Under what input conditions is the output of a 2 input OR gate LOW? Under what input conditions is the output of a 2 input AND gate HIGH?**

 *A two input OR gate is LOW when both inputs, A and B, are 0 or LOW. A two input AND gate is HIGH when both inputs, A and B, are 1 or HIGH.*

**3. We are given a 3 input AND gate and want to use it as a 2 input AND gate. Two inputs to the AND gate are connected to the two input signals. How would you connect the third gate input?**

 *The third gate must be put as 1 or HIGH as an input, because it would not affect the output unless are inputs are HIGH and ensure the same result as a two input AND gate.*

**4. If one input to a 3 input OR gate were accidentally connected to VCC (shorted to VCC), how would the output of the OR gate react no matter what the other 2 input levels might be?**

 *The output would always result in HIGH, or 1 , due to the fact that an OR gate would yield HIGH as long as one input is HIGH, or 1.*

**5. If one input to a 3 input AND gate were accidentally connected to Ground (shorted to Ground), how would the output of the AND gate react no matter what the other 2 input levels might be?**

 *The output would always yield LOW,(0), because an AND gate required all inputs to be HIGH,(1), to yield an output of HIGH.*

Conclusion:

In this laboratory exercise we designed circuits utilizing the following logic gates: NOT, OR, and AND. After designing each gate we introduced various inputs and recorded each outcome in their respective data tables. After collecting the data in regards to the outputs to their respective inputs, we were able to deduce the characteristics of each gate and their corresponding boolean expressions.