

**EXPERIMENT #3: NAND and NOR Gates**

**Name:** \_\_\_\_\_ **Date:** \_\_\_\_\_

**Equipment/Parts Needed:**

- 5V DC Power Supply
- Digital Trainer (Logic Probe)
- Breadboard
- DIP Switch
- 7400 (NAND gate)
- 7402 (NOR gate)

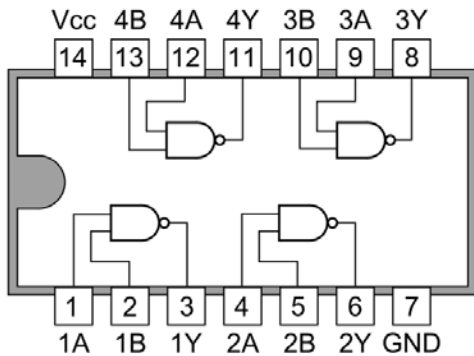
**Objective:**

- To investigate the operation of the **NAND** and **NOR** Gates.
- To form other basic gates using the **NAND** and **NOR** Gates.

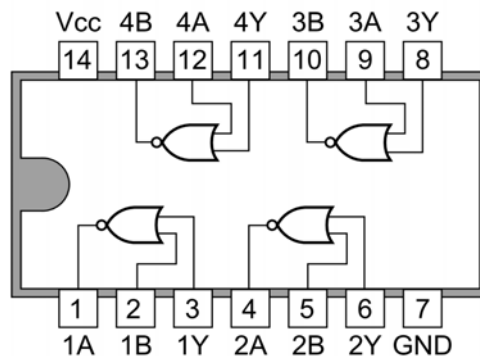
**Discussion:**

- **NAND and NOR** gates are two important gates because they are considered universal gates. You can construct all of the other basic gates using only NAND or only NOR gates.
- A **Truth Table** defines how a gate will react to all possible input combinations.
- A Logic Probe is a piece of test equipment which displays the logic level at a point in the circuit. 0 to 0.8V = Logic 0 and lights the **L** indicator. 2.0V to 5.0V = Logic 1 and lights the **H** indicator. Invalid logic voltage levels light neither indicator.

7400 Quad 2-input NAND Gates



7402 Quad 2-input NOR Gates



## EMT1250 LABORATORY EXPERIMENT

### Part 1: The NAND gate

1. Construct the circuit shown in Figure 3-1 using one gate in the 7400 QUAD NAND GATE (Note that VCC and GND connections are not shown). Use two sections of the DIP switch to set the inputs to 0 or 1 and fill in the Truth Table with the output logic levels. Use the Logic Probe to determine logic levels.

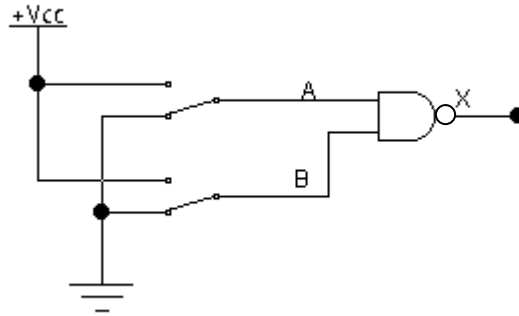


Figure 3-1 Schematic for NAND gate

A	B	X	Volts measured
0	0		
0	1		
1	0		
1	1		

Table 3-1 Truth table for Figure 3-1

2. Disconnect the B switch and connect the two inputs together for the NAND gate as shown in Figure 3-2. Determine the truth table for this configuration using the Logic Probe.

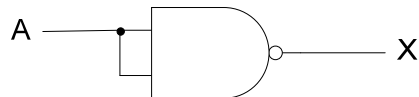


Figure 3-2 NAND gate with inputs connected together

A	X	Volts measured
0		
1		

Table 3-2 Truth table for Figure 3-2

# EMT1250 LABORATORY EXPERIMENT

3. Using two NAND gates, connect the circuits shown in Figure 3-3. Pin numbers are frequently not shown in logic diagrams, so you will need to assign the pin numbers based on the pinout given for the 7400. Determine the truth table for the combination in Table 3-3.

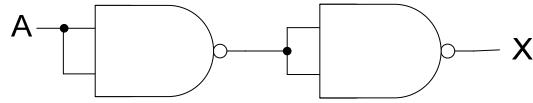


Figure 3-3 Two NAND gates in series with inputs connected together

A	X	Volts measured
0		
1		

Table 3-3 Truth table for Figure 3-3

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**Part 3: The NOR gate**

1. Construct the circuit shown below using one gate in the 7402 QUAD NOR GATE (Note that VCC and GND connections are not shown). Use two sections of the DIP switch to set the inputs to 0 or 1 and fill in the Truth Table with the output logic levels. Use the Logic Probe to determine logic levels.

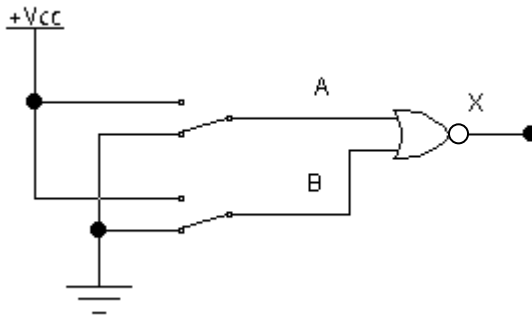


Figure 3-4 Schematic for NOR gate

A	B	X	Volts measured
0	0		
0	1		
1	0		
1	1		

Table 3-4 Truth table for Figure 3-4

2. Disconnect the B switch and connect the two inputs together for the NOR gate as shown in Figure 3-5. Determine the truth table for this configuration using the Logic Probe.

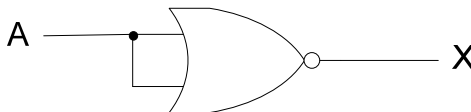


Figure 3-5 NOR gate with inputs connected together

A	X	Volts measured
0		
1		

Table 3-5 Truth table for Figure 3-5

## EMT1250 LABORATORY EXPERIMENT

3. Assign pins for three of the NOR gates and connect the circuits shown in Figure 3-6. Pin numbers are frequently not shown in logic diagrams, so you will need to assign the pin numbers based on the pinout given for the 7402. Determine the truth table for the combination in Table 3-6.

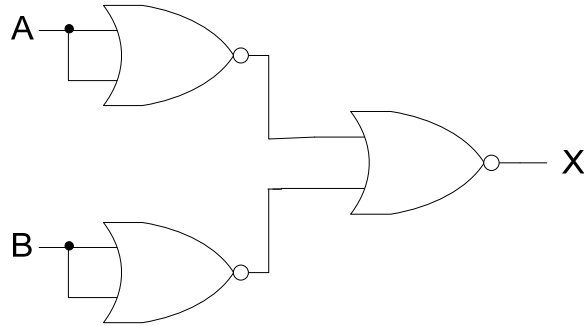


Figure 3-6 Three NOR gates

A	B	X	Volts measured
0	0		
0	1		
1	0		
1	1		

Table 3-6 Truth table for Figure 3-6

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## EMT1250 LABORATORY EXPERIMENT

### Questions/Report:

1. What are the Boolean expressions for the NAND and NOR gates?
2. How does a NAND gate differ from an AND gate?
3. How does a NOR gate differ from an OR gate?
4. Under what input conditions is the output of a 2 input NOR gate LOW? Under what input conditions is the output of a 2 input NAND gate HIGH?
5. From the data in the experiment, how can you configure a NAND or NOR gate to function like an inverter?