CET4805 **Component and Subsystem Design II**

EXPERIMENT # 2: VHDL(VHSIC Hardware Descriptive Language)

Name: _____Date: _____

Equipment/Parts Needed:

Quartus II[R] Web Edition V9.1 SP2 software by Altera Corporation
USB drive to save your files

Objective:

- Learn how to create and modify a VHDL text file and symbol file

Discussion:

VHDL is a high-level, modular language first defined by the IEEE Std 1076-1987. This standard has been revised by IEEE Std 1076-1993 and again by IEEE Std 1076.3-1997. The V in the acronym VHDL represents Very High Speed Integrated Circuit (VHSIC) and HDL stands for Hardware Descriptive Language. Any text editor can be used to create VHDL Design Files Files (.vhd); however it is recommended to use the Quartus II Text Editor to take advantage of features unique to this editor, including syntax coloring of reserved words and comments, error detection, and VHDL templates.

From the Text Editor, a Block Symbol file (.bsf) is created (**File – Create/Update – Create Symbol File For Current File**) that can be included into any Block Design file (.bdf). Altera's version of VHDL, (**AHDL Include File.inc**) can be created and placed into Text Design files (.tdf); however, this lab manual only focuses on VHDL files. VHDL Design files can contain any combination of primitives, megafunctions, macrofunctions, and user defined functions integrated into hierarchical projects.

By no means will you become an expert in writing VHDL files after completing the VHDL labs in this manual. VHDL is only introduced as a means to modularize hardware designs using software. The entire behavior of hardware circuits are encoded in software and due to the densities of today's ASICs (Application Specific Integrated Circuits), FPGAs (Field Programmable Gate Arrays), and CPLDs (Complex Programmable Logic Devices), the only way to manipulate the hardware is through software. Students seeking Associate and Baccalaureate degrees should learn how to read, interpret, modify, compile, and verify basic VHDL design files.

New toolbar icons associated with the Text Editor are shown in Figure 2-1.

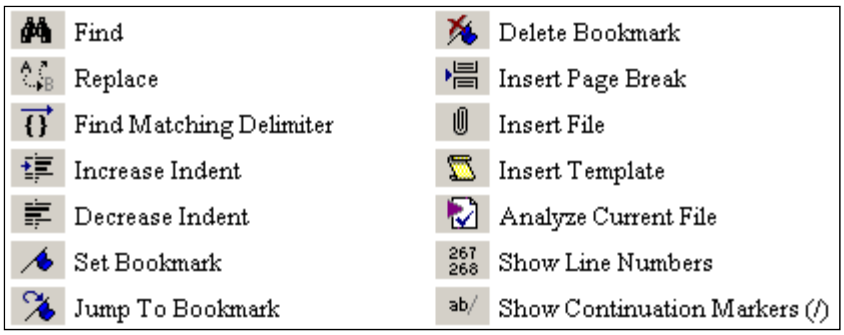

Figure 2-1

Part 1 Procedure

Creating a New Project

1. Open the Quartus II software. Select **File – New Project Wizard**. Enter the appropriate drive letter for the designated storage area on the computer you are using followed by the working directory C**:\altera\91sp2\quartus\kwon\Lab2**. You need to go through the step from 1 through 8 in the Part 1 of **Lab1** manual. Don't forget to create the folder **Lab2** under the subfolder of your last name. Assign the project name **Lab2_1 (**Figure 2-2**)**, assign ***Cyclone II*** for the device family, and select the ***EP2C35F672C6*** chip in the Family & device settings [page of 3 of 5].

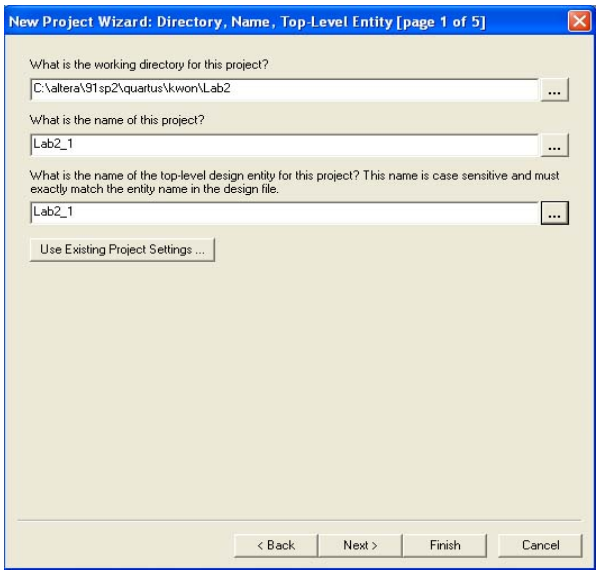

Figure 2-2

Creating a VHDL File (bdf)

2. Open a new VHDL Device Design file (**File > New**) by highlighting VHDL File. And click OK. A Text Editor opens titled Vhdl1.vhd* with the first line numbered in light gray text. Type the VHDL code shown in Text Box 1. All reserved words will appear as blue text, comments are green, and all other characters will be black. Reserved words shown in Text Box 1 are in capital letters; however, **VHDL is not case sensitive**.

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY vhdl_1 IS
      PORT(
            A, B  :IN std_logic;
            AandB :OUT std_logic);
END vhdl_1;
ARCHITECTURE behavior OF vhdl_1 IS
      BEGIN
            AandB <= a AND b;       -- AND is a reserved word
END behavior;
```

Text Box 1

3. Save the VHDL file as **vhdl_1.vhd** as part of our project under your subfolder. Place a check mark in the space labeled Add file to current project and press Save (See Figure 2-3).

4. Select **File – Create/Update – Create Symbol Files for Current File** to create a symbol file for the VHDL code entered. A Compilation Report window initially displays “Report not available”; however, be patient. A display window should soon appear stating that the **Create Symbol File was (or not) successful**. Click **OK** and close the Compilation Report window.

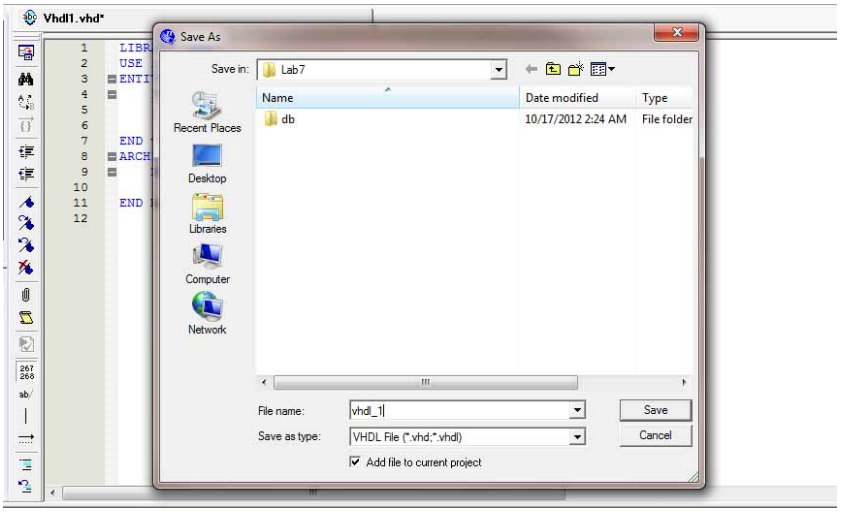

Figure 2-3

5. The compiler should display the successful message. If you made typographical errors, the compiler messenger (see the Messages Utility Window at the bottom of the screen) will identify each error and pinpoint the line the error occurs on or near. Double-click on the (red) errors, starting with the first one on the list, and correct all typographical errors.

6. Once the errors have been corrected, save the file (**File - Save**) and again try to create a default symbol. When you try to create a symbol for the second time, the software prompts you to overwrite the existing file. Click on **OK** to continue. If unsuccessful, correct all typographical errors and repeat this step until the **Create Symbol File was successful**. Click **OK** then close the Compilation Report window.

7. Open a new Schematic file (**File > New**) by highlighting **Block Diagram/Schematic File**. And click **OK**.

8. Either click on the two input AND gate symbol in the Block Diagram File toolbar or double click in the Block1.bdf work area to open the Symbol window. Two libraries are shown, Project and c:/altera/91sp2/quartus/libraries. (See Figure 2-4.) Click on the + sign to expand the Project library, revealing the vhdl_1symbol file just created. Double-click on the vhdl_1symbol file name and place the symbol in the center of the work area. Add input and output symbols and wire accordingly to create the schematic shown in Figure 2-5.

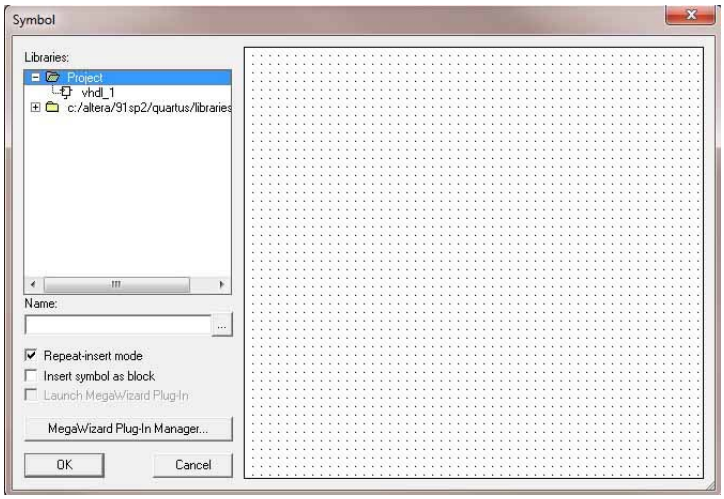

Figure 2-4

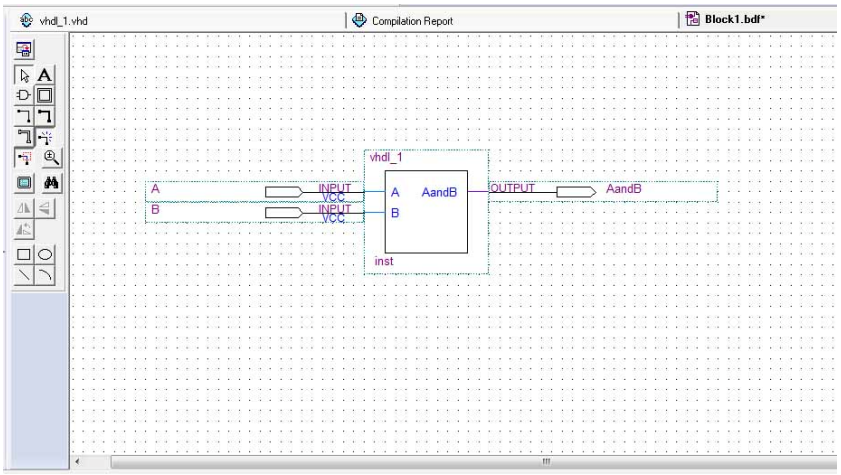

Figure 2-5

9. Before compiling this *bdf* file, we need to name this *bdf* file and save it as part of our project under your subfolder. Choose **File > Save As** and enter **File name** as *lab2_1*. Place a *check mark* in the space labeled **Add file to current project** and press **Save**.

10. Compile the project by selecting **Processing** > **Start Compilation**, or press Ctrl-L, or use the Compilation button in the toolbar. The compilation takes several seconds. When it is complete it should give a message that indicates, "Full compilation was sucessful". Press **OK**. If unsuccessful, correct all errors and try to re-compile.

Simulating a Vector Waveform File (vwf)

11. As you have done step 23 through 28 in the **Part 1** of Lab1, you need to create a **Vector Waveform File (*vwf*)** to simulate a design(*bdf*) file. Add all inputs and output, specify an end time of 16 µs and a grid size of 1µs for our waveform display, and then save it as lab2_1.vwf.

12. Select **Processing – Start Simulation**, or press Ctrl-I, or use the Simulation button in the toolbar. After a few moments a message stating "Simulation was successful" should appear. Click **OK**.

13. The Simulation Waveforms appear in the Simulation Report shown in the Figure 2-6. You may have to expand the size of the Simulation Waveforms to suit your need and choose **View > Fit in Window** to see the entire 16µs waveform.

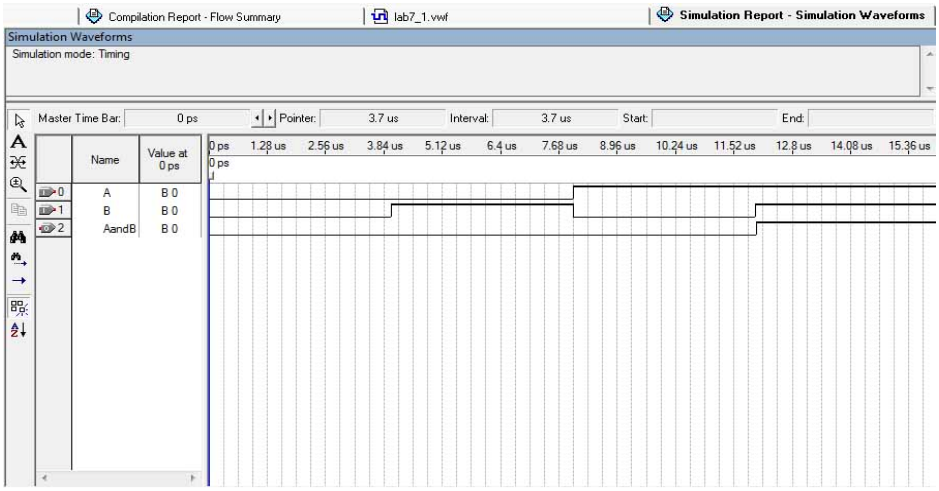

Figure 2-6

14. Compare the simulation result with that of the *lab1_1.vwf*.

Part 2 Practice

1. Use Quartus II software to design the Boolean equation $X = A\overline{B} + C$.
   1) Design a VHDL File (*vhdl* file) for X.
   2) Create a Block Design File (*bdf* file) for X using the symbol created from the *vhdl* file.
   3) Create a Vector Waveform File (*vwf*) for X. The simulation should show all possible combination of inputs.
   4) Compare the result of the vector waveform with that of Lab1.
   5) Include the copies of *vhdl* and *bdf* files and *vwf* file in the lab report.

A	B	C	X
0	**0**	**0**	
0	**0**	**1**	
0	**1**	**0**	
0	**1**	**1**	
1	**0**	**0**	
1	**0**	**1**	
1	**1**	**0**	
1	**1**	**1**	

Table 2-2 Truth table

Instructor's Signature:_____, Date: _____

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2. Use Quartus II software to design the Boolean equation $Y = A\overline{B} + \overline{C}D$.

1) Design a VHDL File (*vhdl* file) for Y.
2) Create a Block Design File (*bdf* file) for Y using the symbol created from the *vhdl* file.
3) Create a Vector Waveform File (*vwf*) for Y. The simulation should show all possible combination of inputs.
4) Compare the result of the vector waveform with that of Lab1.
5) Include the copies of *vhdl* and *bdf* files and *vwf* file in the lab report.

A	B	C	D	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Instructor's Signature:_____, Date: _____